1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MLB_BAFFIN,X363G

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
10	0006897289	ENGINEERING RELEASED	2016-08-24

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29	30	USB-C Support	X363_AGOTETI	08/08/2016
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91	100	BAFFIN PCI-E	X363_SEAN	01/27/2016
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DRAWING
TITLE=MLB_BAFFIN
ABBREV=ABBREV
LAST_MODIFIED=Wed Aug 24 09:57:44 2016

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00647	1	SCHEM,MLB-BAFFIN,X363G	SCH	CRITICAL	
820-00281	1	PCBF,MLB-BAFFIN,X363G	PCB	CRITICAL	

LAST_MODIFICATION=Wed Aug 24 09:57:44 2016

This is the PVT design

DRAWING TITLE
SCHEM,MLB-BAFFIN,X363

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DRAWING NUMBER 051-00647 SIZE D
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00076	COMMON PARTS,MLB-BAFFIN,X363	X363_COMMON
985-00126	DEV,MLB-BAFFIN,X363	X363_DEVEL:PVT
985-00232	DEV,MLB-BAFFIN,PVT,X363	X363_DEVEL:PVT

639 BOMs have been moved to the end of the schematic

GPU Options

BOM GROUP	BOM OPTIONS
2GB_MC_BAFFIN	FB_2GB_MICRON,VRAM:GRP1
2GB_HY_BAFFIN	FB_2GB_HYNIX,VRAM:GRP1
2GB_SM_BAFFIN	FB_2GB_SAMSUNG,VRAM:GRP2
4GB_SM_BAFFIN	FB_4GB_SAMSUNG,VRAM:GRP1
4GB_MC_BAFFIN	FB_4GB_MICRON,VRAM:GRP1

FB VDRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00044	4	IC,GDDR5,4Gb,7Gbps,1.5V,25NM,A,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_2GB_MICRON
333S00043	4	IC,GDDR5,4Gb,7Gbps,1.5V,25NM,A,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_2GB_HYNIX
333S00078	4	IC,GDDR5,8Gb,7Gbps,1.5V,25NM,B,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_2GB_SAMSUNG
333S00074	4	IC,GDDR5,8Gb,7Gbps,1.5V,25NM,B,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_4GB_SAMSUNG
333S00075	4	IC,GDDR5,8Gb,7Gbps,1.5V,25NM,A,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_4GB_MICRON

Sub-BOM DIPLEXER

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00085	DIPLEXERS,MURATA,X363G	DIPLEXER:MURATA

X363 BOM Groups

BOM GROUP	BOM OPTIONS
X363_COMMON	ALTERNATE,COMMON,X363_COMMON1,X363_COMMON2,X363_COMMON3,X363_COMMON4,X363_PROGPARTS
X363_COMMON1	SOC:HYNIX,SE:PROD,SKIP_5V3V3:AUDIBLE,DIPLEXER:MURATA,T208_PROG:REV5,BOARD_ID:17,VCCHDA:S0
X363_COMMON2	XDP:YES,SAMCONN,SOC_BOOT:SPI,DPMUX_XTAL:NO,GPUCLK:OSC,BAFFIN,AP_TEMP,VCCPLLOC:S3,WIFI_SAK:NO
X363_COMMON3	CPUTHRM:ALRT,TBTTHRM:ALRT,LOADRC:NO,OTHERRC:YES,DDRRC:YES,TBTRC:YES,TPADRC:YES,LID_FEATURE_ON
X363_COMMON4	EDP:YES,CPUPEG:X8X4X4,TBTTHRM_SNS,GPUTHRM_SNS,S3_STATE:YES,GPU_ROM:YES,SVID_PU:CORE
X363_PROGPARTS	BOOTROM_PROG:DVT,BT_PROG:DVT,WIFI_PROG:DVT,UPCROM_PROG:DVT,SMC_PROG:PVT,DPMUXMCU:PROG,PCC:NO
X363_DEVEL:ENG	ALTERNATE,ENGISNS,DBGLED,XDP_CONN,USBC_DBG,DBG_BTN,DBG_FAN,DBG_XTAL,DPMUX_DEBUG,WIFI_DBG,SSD_DEBUG,GPUROM:BLANK,PCC:YES
X363_DEVEL:DVT	ALTERNATE,ENGISNS,DBGLED,XDP_CONN,USBC_DBG,DBG_BTN,DBG_FAN,DBG_XTAL,DPMUX_DEBUG,WIFI_DBG,SSD_DEBUG
X363_DEVEL:PVT	ALTERNATE,XDP_CONN,USBC_DBG
ENGISNS	TBTISNS,LOADISNS,TPADISNS,DDRISNS,OTHERISNS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00227	1	CPU,SKY,SR2FT,R1,PRQ,4/2,2.9,BGA1440	U0500	CRITICAL	CPU_SKL:2.9
337S00228	1	CPU,SKY,SR2FU,R1,PRQ,4/2,2.7,BGA1440	U0500	CRITICAL	CPU_SKL:2.7
337S00229	1	CPU,SKY,SR2FQ,R1,PRQ,4/2,2.6,BGA1440	U0500	CRITICAL	CPU_SKL:2.6
998-04701	1	INTERPOSER,INTEL,BGA1440,MM940989	U0500	CRITICAL	CPU_SKL:SOCKET
337S00258	1	IC,SKL PCH-H,SFF,SR2NH,PRQ,D1,BGA939	U1100	CRITICAL	
353S00961	4	IC,CD3215,ACE,C0,USB PWR SW,BLNK,BGA96	U3100,U3200,UB300,UB400	CRITICAL	
338S00254	2	IC,TBT,ALPINE RIDGE DP,QT5S,QS,C1,BGA337	U2800,UB000	CRITICAL	
353S01016	1	IC,ISL9239HIZ,PMU,TUBA,WCSP40,2.1X3.3MM	U7000	CRITICAL	
338S00221	1	IC,PMU,P650839,7X7MM.BGA168	U7800	CRITICAL	
338S00142	1	IC,CODEC,CLIFDEN,CS42L83A,B0,WLCSP49	U6300	CRITICAL	
337S00330	1	IC,GPU,BAFFIN,ULA,A1,PS,BGA769	UA000	CRITICAL	BAFFIN_ULA
337S00331	1	IC,GPU,BAFFIN,PROA,A1,PS,BGA769	UA000	CRITICAL	BAFFIN_PROA
337S00332	1	IC,GPU,BAFFIN,LEA,A1,PS,BGA769	UA000	CRITICAL	BAFFIN_LEA
998-04866	1	INTERPOSER,AMD,C989,BGA769,VDDCI/MVDD	UA000	CRITICAL	STARDUST:VDDCI_MVDD
998-04867	1	INTERPOSER,AMD,C988,BGA769,VDDC	UA000	CRITICAL	STARDUST:VDDC
677-04532	2	SUBASSY (T&R) PCBA, AMR, INTERPOSER, X363	J5250,J5260	CRITICAL	

Development/Base BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00076	1	COMMON PARTS,MLB-BAF,X363	BASE	CRITICAL	BASE_BOM
985-00126	1	DEV,MLB-BAF,X363	DEVEL	CRITICAL	DEVEL_BOM

WIFI/BT Diplexers

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
155S0979	3	FLTR,DIPLEXER,2.45/5.54GHZ,0805	U3810,U3820,U3830	CRITICAL	DIPLEXER:MURATA

Main DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00050	4	IC,SDRAM,LPDDR3-2133,32GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	16G_SAMSUNG_2133
333S00070	4	IC,SDRAM,LPDDR3-2133,32GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	16G_MICRON_2133

Main DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM_16G_SAMSUNG_2133	16G_SAMSUNG_2133,RAMCFG4:L,RAMCFG3:L,RAMCFG0:L
RAM_16G_MICRON_2133	16G_MICRON_2133,RAMCFG4:L,RAMCFG3:L,RAMCFG1:L

Strategic Silicon

PART#	STRATEGIC VALUE	COMMENT
337S00227	08	CPU
337S00228	08	CPU
337S00229	08	CPU
333S00050	07	MAIN MEMORY
333S00070	07	MAIN MEMORY
335S00149	02	SSD NAND
335S00204	02	SSD NAND
335S00205	02	SSD NAND
335S00219	02	SSD NAND
339S00154	02	SSD CONTROLLER
339S00155	02	SSD CONTROLLER
338S00166	02	SSD PMIC
337S00225	08	GPU
337S00285	08	GPU
337S00286	08	GPU
333S00044	07	VIDEO MEMORY
333S00043	07	VIDEO MEMORY
333S00078	07	VIDEO MEMORY
333S00074	07	VIDEO MEMORY
333S00075	07	VIDEO MEMORY
343S00135	10	T208
343S00136	10	T208
343S00137	10	T208
338S00138	10	T208
338S00193	09	BERKELIUM
353S3978	02	MOJAVE
338S00097	02	SECURE ELEMENT
338S00254	08	ALPINE RIDGE
353S00961	09	ACE
338S00142	09	CLIFDEN
353S00604	07	AUDIO AMP
353S4316	08	BAYSIDE
338S00221	08	BANJO
353S00853	09	TUBA
339S00056	05	ICEBOCK
359S00006	08	GREEN CLOCK
353S00795	09	DEBUG MUX

SYNC_MASTER=J80_MLB SYNC_DATE=07/07/2015

PAGE TITLE
BOM Configuration

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Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
338S1231	1	IC,SMC12,40MHZ/50DMIPS MCU,7X7,168BGA	U5000	CRITICAL	SMC_PROG:BLANK	Blank
341S00701	1	IC,SMC-B1,EXT (v2.37F7) PVT,X363G	U5000	CRITICAL	SMC_PROG:PVT	TI
335S00013	1	IC,SPI SERIAL FLASH,64M BITS,3V,8P SOIC,QE=1	U6100	CRITICAL	BOOTROM_PROG:BLANK	Blank
341S00699	1	IC,EFI ROM (V0193), DVT, X363G	U6100	CRITICAL	BOOTROM_PROG:DVT	Macronix/Winbond
353S00926	2	IC,CD3215,ACE,B03,BLNK,BGA96	U2890,UB090	CRITICAL	UPCROM_PROG:BLANK	Blank
341S00707	1	T29,AR1 (V10.5) PVT, X363G	U2890	CRITICAL	UPCROM_PROG:DVT	Winbond
341S00708	1	T29,AR2 (V10.5) PVT, X363G	UB090	CRITICAL	UPCROM_PROG:DVT	Winbond
335S00024	1	IC,SERIAL-FLASH,2MBIT,4V,8-USON,2x3x,6MM	U3750	CRITICAL	BT_PROG:BLANK	Blank
341S00695	1	IC,BT ROM (V28), DVT, X362/X363	U3750	CRITICAL	BT_PROG:DVT	Macronix/Winbond
341S00709	1	WIFI ROM (P107) DVT,NEW,WW1,X362/X363	U3710	CRITICAL	WIFI_PROG:DVT	Rohm/On Semi
341S3565	1	IC, EDP MUX-95C, (RENESAS) V3.2.8,DVB,D2	U9800	CRITICAL	DPMUXMCU:PROG	
335S0724	1	IC,1Mbit SERIAL FLASH 2X3X0.6MM UFDFPN8 PKG	UA701	CRITICAL	GPUROM:BLANK	Blank

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Pogo Pins

APN 870-01771
PG0410
POGO-2.30D-4.63H-SM
SM

PG0411
POGO-2.30D-4.63H-SM
SM

PG0420
POGO-2.30D-4.63H-SM
SM

PG0421
POGO-2.30D-4.63H-SM
SM

PG0430
POGO-2.30D-4.63H-SM
SM

PG0471
POGO-2.30D-4.63H-SM
SM

PG0470
POGO-2.30D-4.63H-SM
SM

APN 870-01772
PG0400
POGO-2.30D-4.06H-SM
SM

PG0401
POGO-2.30D-4.06H-SM
SM

SMT Bosses

APN 860-00392
BS0400
3.40D1.75ID-1.12H-SM
USB-C Left
BOT side - North

BS0401
3.40D1.75ID-1.12H-SM
USB-C Left
BOT side - South

BS0410
3.40D1.75ID-1.12H-SM
USB-C Right
BOT side - North

BS0411
3.40D1.75ID-1.12H-SM
USB-C Right
BOT side - South

APN 806-06520
BS0420
3.40D1.75ID-1.45H-SM
DFR Touch
BOT side

APN 806-06600
BS0480
3.40D1.75ID-2.12H-SM
USB-C Right
BOT side - Left

APN 806-06521
BS0430
3.40D1.75ID-1.9H-SM
DFR Display
BOT side - Left

BS0431
3.40D1.75ID-1.9H-SM
DFR Display
BOT side - Right

BS0440
3.40D1.75ID-1.9H-SM
Keyboard
BOT side - Left

BS0441
3.40D1.75ID-1.9H-SM
Keyboard
BOT side - Right

BS0450
3.40D1.75ID-1.9H-SM
Trackpad
BOT side - Left

BS0451
3.40D1.75ID-1.9H-SM
Trackpad
BOT side - Right

APN 860-00413
BS0460
3.40D1.75ID-1.57H-SM
Lifeboat
BOT side - North

BS0461
3.40D1.75ID-1.57H-SM
Lifeboat
BOT side - South

APN 860-00469
BS0470
2.7X1.8R-1.4ID-0.91H-SM
eDP
TOP side - Left

BS0701
2.7X1.8R-1.4ID-0.91H-SM
eDP
TOP side - Right

APN 806-07958
TOUCH-COWLING-HOOK-X378
BS0704
SM
DFR Touch - TOP side

Rubber Mount Standoffs

APN 860-00452
BM0400
3.090D1.4ID-3.25H-SM

APN 860-00435
BM0401
2.80D1.2ID-1.55H-SM

BM0402
2.80D1.2ID-1.55H-SM

BM0403
2.80D1.2ID-1.55H-SM

BM0404
2.80D1.2ID-1.55H-SM

BM0405
2.80D1.2ID-1.55H-SM

BM0406
2.80D1.2ID-1.55H-SM

BM0407
2.80D1.2ID-1.55H-SM

BM0408
2.80D1.2ID-1.55H-SM

BM0409
2.80D1.2ID-1.55H-SM

BM0410
2.80D1.2ID-1.55H-SM

BM0411
2.80D1.2ID-1.55H-SM

BM0483
2.80D1.2ID-1.55H-SM

APN 860-00500
BM0484
2.80D1.2ID-3.5H-SM

APN 860-00500
BM0485
2.80D1.2ID-3.5H-SM

BM0486
2.80D1.2ID-3.5H-SM

BM0487
2.80D1.2ID-3.5H-SM

Shield Can TH

APN 998-2691
TH0400 — System Memory - BOT side - Left
TH0401 — System Memory - BOT side - Right
TH0410 — TBT Left - BOT side - North
TH0411 — TBT Left - BOT side - South
TH0420 — TBT Right - BOT side - North
TH0421 — TBT Right - BOT side - South
TH-NSP
SL-1.1X0.4-1.4X0.7

T208 - TOP side - North

T208 through holes are non-plated... for now

T208 - TOP side - South

TH0440 — SSD - BOT side - North
TH0441 — SSD - BOT side - South
TH0450 — SSD - TOP side - North
TH0451 — SSD - TOP side - South

TH0460 — Frame Buffer Memory - BOT side - Left
TH0461 — Frame Buffer Memory - BOT side - Right

Shield Can Fence

SH0400 — OMIT_TABLE — DRAM - BOT side — APN 806-06590
SH0410 — OMIT_TABLE — AR Right - BOT side — APN 806-06586
SH0420 — OMIT_TABLE — AR Left - BOT side — APN 806-06588
SH0430 — T208 - TOP side — APN 806-07814
SH0440 — OMIT_TABLE — SSD - TOP side — APN 806-06584
SH0450 — OMIT_TABLE — SSD - BOT side — APN 806-06585
SH0460 — OMIT_TABLE — Diplexer - BOT side — APN 806-06591
SH0470 — OMIT_TABLE — VRAM - BOT side — APN 806-08026
SM
SHLD-FENCE-MLB-M8-X379
SHLD-FENCE-M8-X379

Shield Can Omit Table

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-08023	1	SHIELD,FENCE,DRAM,X378	SH0400	CRITICAL	
806-08019	1	SHIELD,FENCE,ALPINE RIDGE,RIGHT,X378	SH0410	CRITICAL	
806-08021	1	SHIELD,FENCE,ALPINE RIDGE,LEFT,X378	SH0420	CRITICAL	
806-07918	1	SHIELD,NAND,TOP,ALT,X363	SH0440	CRITICAL	
806-07917	1	SHIELD,NAND,BOTTOM,ALT,X363	SH0450	CRITICAL	
806-08024	1	SHIELD,DIPLEX,EG,X378	SH0460	CRITICAL	
806-08026	1	FENCE,VRAM,EG,X378	SH0470	CRITICAL	

BOM_COST_GROUP=MECHANICALS

SYNC_MASTER=J80_MLB SYNC_DATE=11/16/2015

PAGE TITLE
PD Parts

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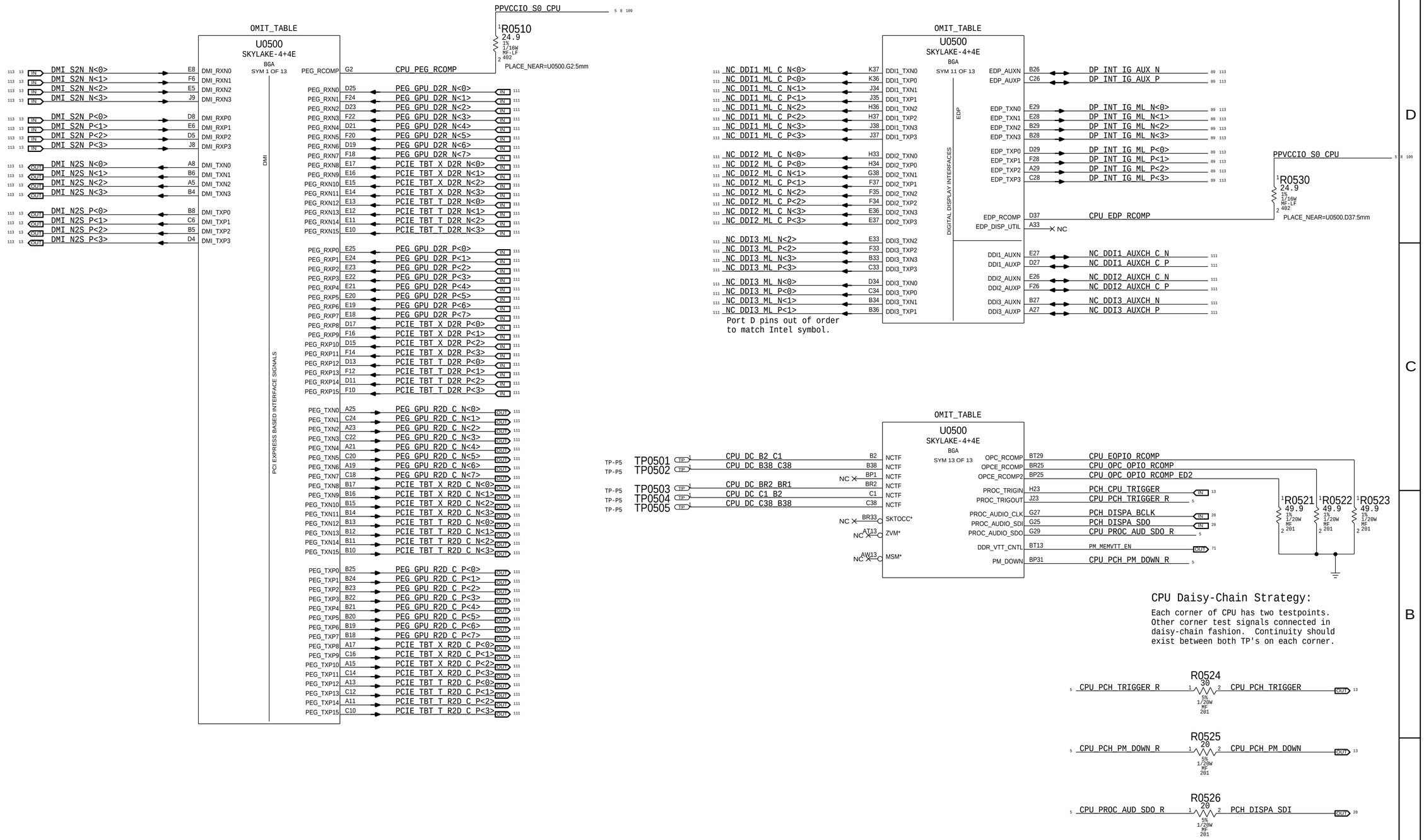

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE

CPU DMI/PEG/FDI/RSVD

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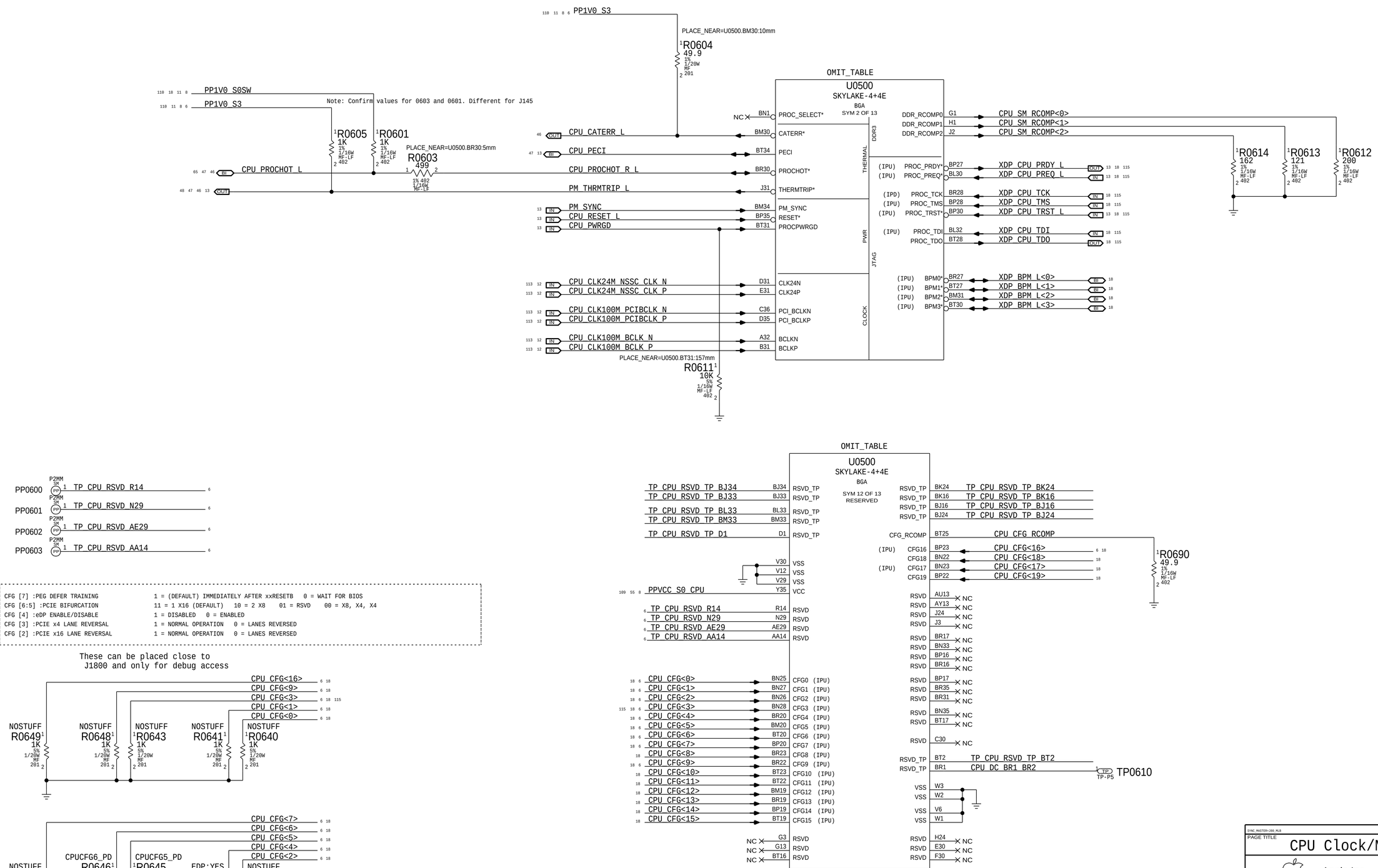

BOM GROUP	BOM OPTIONS
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD,CPUCFG5_PD

To use PEG X16 configuration, simply remove CPUPEG:X8X8 and CPUPEG:X8X4X4 from BOMs.

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
CPU Clock/Misc/JTAG/CFG

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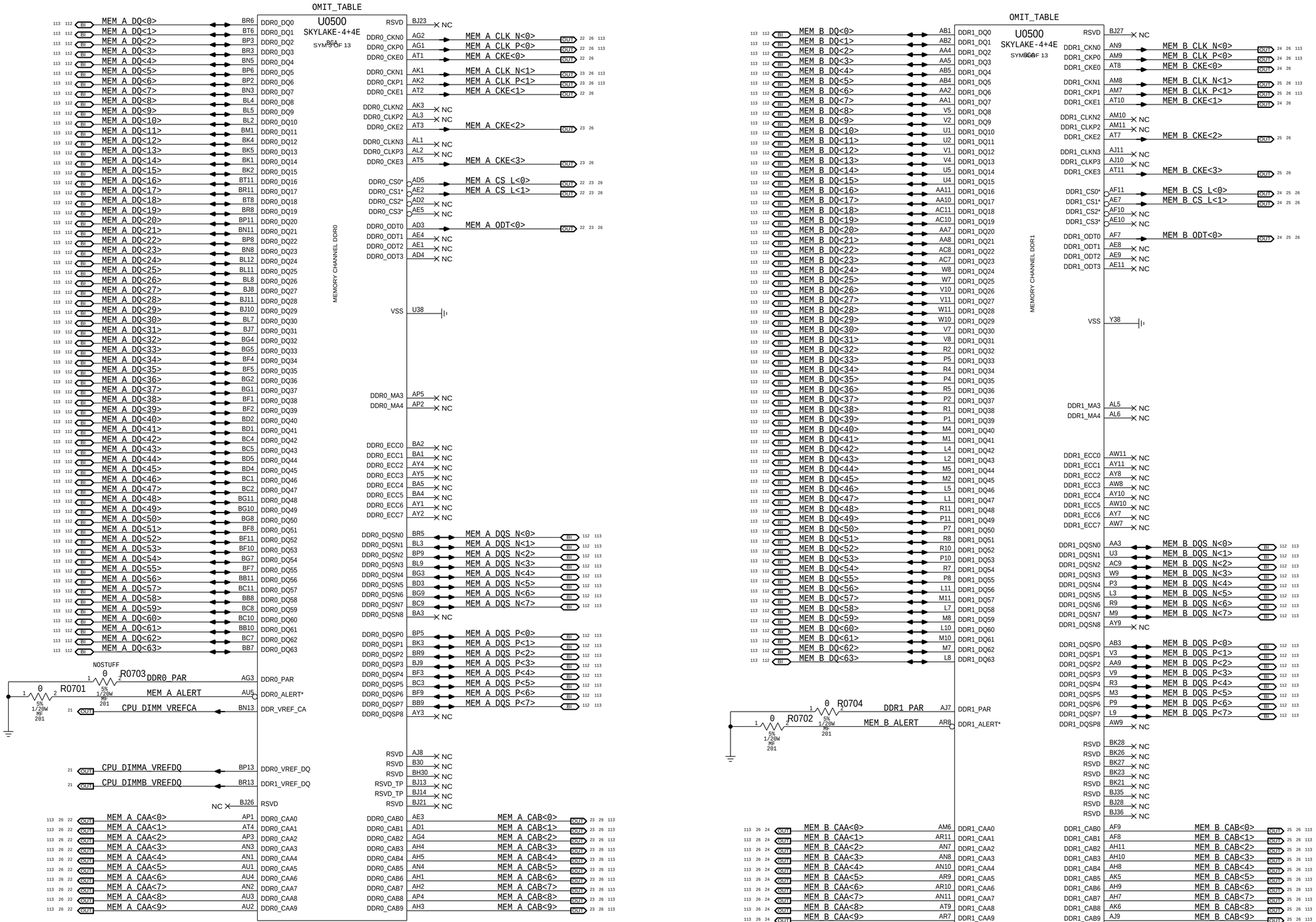

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE

CPU DDR3 Interfaces

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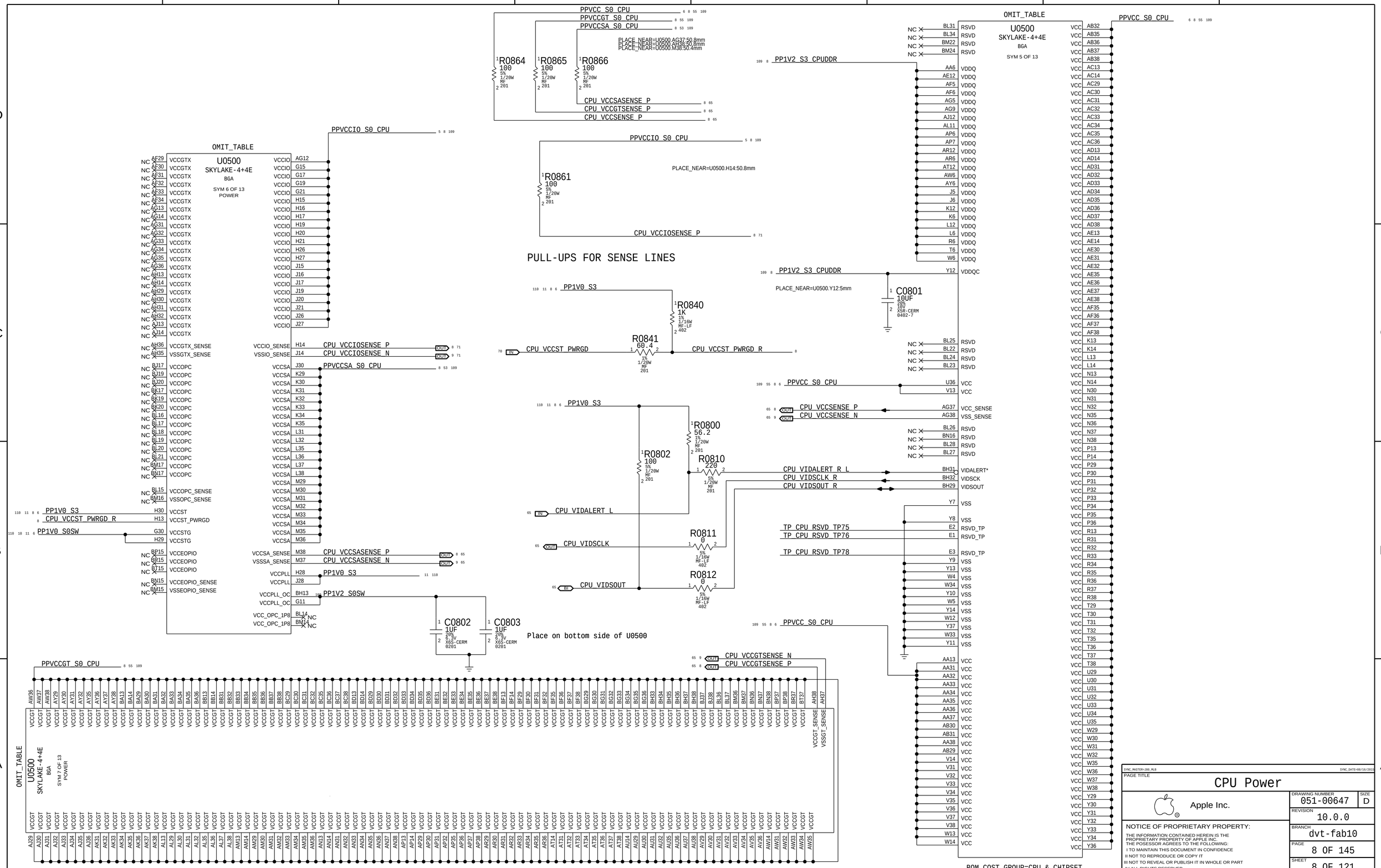
OMIT_TABLE
U0500
SKYLAKE-4+4E
BGA
SYM 6 OF 13
POWER
SYM 5 OF 13
SYM 7 OF 13
PPVCC_S0_CPU
PPVCCGT_S0_CPU
PPVCCSA_S0_CPU
PPVCCIO_S0_CPU
PPV1V2_S3_CPUDDR
PPV1V0_S3
PPV1V0_S0SW
PPV1V2_S0SW
PPVCCGT_S0_CPU
R0864 100 5% 1/20W MF 201
R0865 100 5% 1/20W MF 201
R0866 100 5% 1/20W MF 201
PLACE_NEAR=U0500.AG37:50.8mm
PLACE_NEAR=U0500.AG38:50.8mm
PLACE_NEAR=U0500.N38:50.4mm
CPU_VCCSASENSE_P
CPU_VCCGTSENSE_P
CPU_VCCSENSE_P
R0861 100 5% 1/20W MF 201
PLACE_NEAR=U0500.H14:50.8mm
CPU_VCCIOSENSE_P
PULL-UPS FOR SENSE LINES
R0840 1K 1% 1/16W MF-LF 402
R0841 60.4 1% 1/20W MF 201
CPU_VCCST_PWRGD
CPU_VCCST_PWRGD_R
R0800 56.2 1% 1/20W MF 201
R0802 100 5% 1/20W MF 201
R0810 220 5% 1/20W MF 201
R0811 0 5% 1/16W MF-LF 402
R0812 0 5% 1/16W MF-LF 402
CPU_VIDALERT_L
CPU_VIDSCLK
CPU_VIDSOUT
C0801 10UF 20% 6.3V X5R-CERM 0402-7
PLACE_NEAR=U0500.Y12:5mm
C0802 1UF 20% 6.3V X6S-CERM 0201
C0803 1UF 20% 6.3V X6S-CERM 0201
Place on bottom side of U0500
CPU_VCCSENSE_P
CPU_VCCSENSE_N
CPU_VIDALERT_R_L
CPU_VIDSCLK_R
CPU_VIDSOUT_R
TP_CPU_RSVD_TP75
TP_CPU_RSVD_TP76
TP_CPU_RSVD_TP78
CPU_VCCGTSENSE_N
CPU_VCCGTSENSE_P
CPU_VCCIOSENSE_P
CPU_VCCIOSENSE_N
CPU_VCCSASENSE_P
CPU_VCCSASENSE_N
BOM_COST_GROUP=CPU & CHIPSET
SYNC_MASTER=J80_MLB
SYNC_DATE=08/16/2016
PAGE TITLE
CPU Power
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DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
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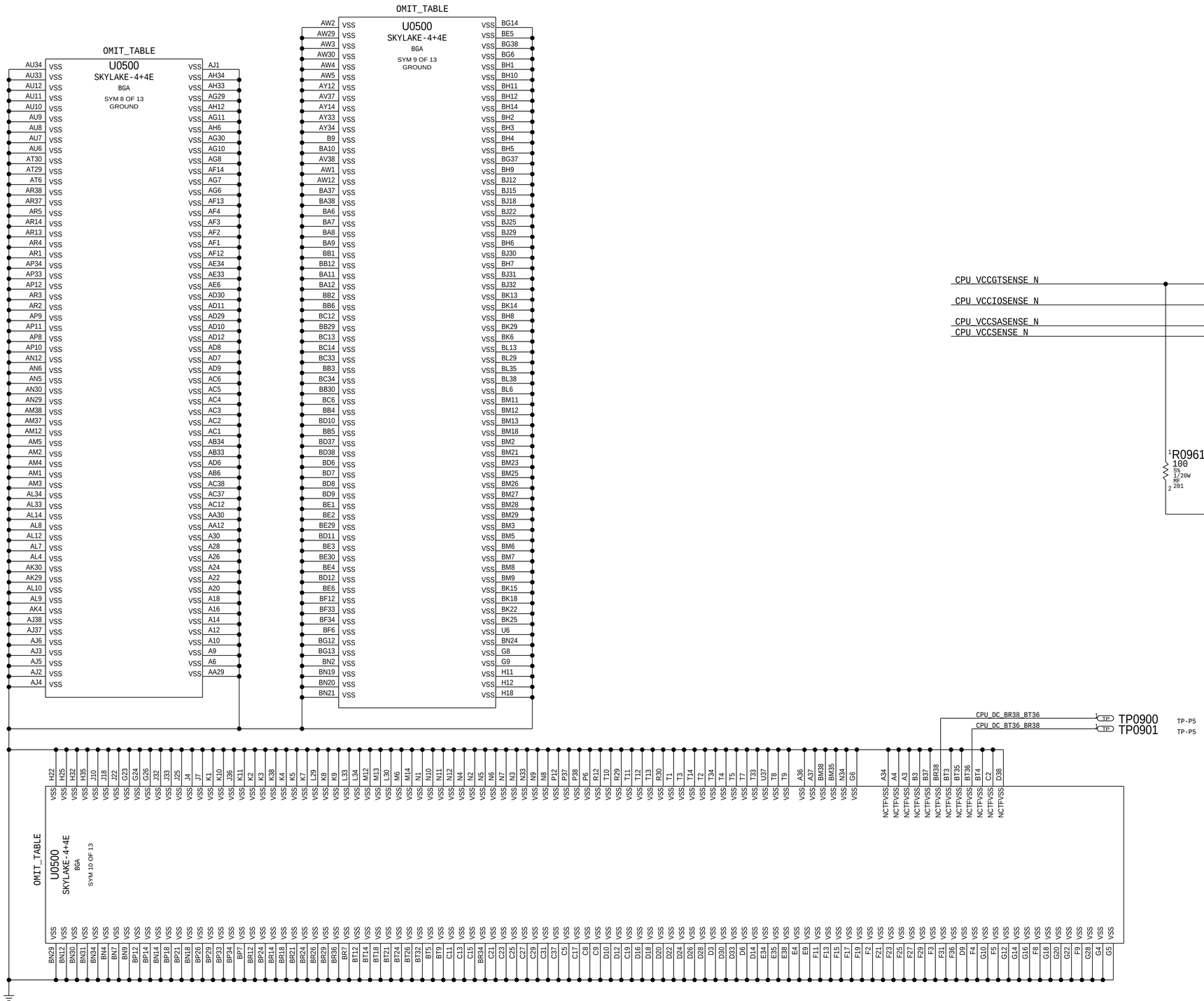

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PAGE TITLE

CPU Ground

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Vcc CPU Core Decoupling from 20140905 BOM

CPU VCORE Decoupling

Intel recommendation: 5x 220uF ESR 5m ohms ESL 1.9nH each,4x 47uF 0805 8x22uF 0603, 28x 10uF 0402, 3x 10uF 0402, 69x 1uF 0201 Board Edge: 2x 220uF, 4x 47uF rest on the back side
Apple Implementation:

109 PPVCC_S0_CPU

Place on bottom side of U0500

C1000 1UF 20% 4V CERM-X6S 0201
C1001 1UF 20% 4V CERM-X6S 0201
C1002 1UF 20% 4V CERM-X6S 0201
C1003 1UF 20% 4V CERM-X6S 0201
C1004 1UF 20% 4V CERM-X6S 0201
C1005 1UF 20% 4V CERM-X6S 0201
C1006 1UF 20% 4V CERM-X6S 0201
C1007 1UF 20% 4V CERM-X6S 0201
C1008 1UF 20% 4V CERM-X6S 0201
C1009 1UF 20% 4V CERM-X6S 0201
C1010 1UF 20% 4V CERM-X6S 0201
C1011 1UF 20% 4V CERM-X6S 0201
C1012 1UF 20% 4V CERM-X6S 0201
C1013 1UF 20% 4V CERM-X6S 0201
C1014 1UF 20% 4V CERM-X6S 0201
C1015 1UF 20% 4V CERM-X6S 0201
C1016 1UF 20% 4V CERM-X6S 0201
C1017 1UF 20% 4V CERM-X6S 0201
C1018 1UF 20% 4V CERM-X6S 0201
C1019 1UF 20% 4V CERM-X6S 0201
C1020 1UF 20% 4V CERM-X6S 0201
C1021 1UF 20% 4V CERM-X6S 0201
C1022 1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1023 1UF 20% 4V CERM-X6S 0201
C1024 1UF 20% 4V CERM-X6S 0201
C1025 1UF 20% 4V CERM-X6S 0201
C1026 1UF 20% 4V CERM-X6S 0201
C1027 1UF 20% 4V CERM-X6S 0201
C1028 1UF 20% 4V CERM-X6S 0201
C1029 1UF 20% 4V CERM-X6S 0201
C1030 1UF 20% 4V CERM-X6S 0201
C1031 1UF 20% 4V CERM-X6S 0201
C1032 1UF 20% 4V CERM-X6S 0201
C1033 1UF 20% 4V CERM-X6S 0201
C1034 1UF 20% 4V CERM-X6S 0201
C1035 1UF 20% 4V CERM-X6S 0201
C1036 1UF 20% 4V CERM-X6S 0201
C1037 1UF 20% 4V CERM-X6S 0201
C1038 1UF 20% 4V CERM-X6S 0201
C1039 1UF 20% 4V CERM-X6S 0201
C1040 1UF 20% 4V CERM-X6S 0201
C1041 1UF 20% 4V CERM-X6S 0201
C1042 1UF 20% 4V CERM-X6S 0201
C1043 1UF 20% 4V CERM-X6S 0201
C1044 1UF 20% 4V CERM-X6S 0201
C1045 1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1046 1UF 20% 4V CERM-X6S 0201
C1047 1UF 20% 4V CERM-X6S 0201
C1048 1UF 20% 4V CERM-X6S 0201
C1049 1UF 20% 4V CERM-X6S 0201
C1050 1UF 20% 4V CERM-X6S 0201
C1051 1UF 20% 4V CERM-X6S 0201
C1052 1UF 20% 4V CERM-X6S 0201
C1053 1UF 20% 4V CERM-X6S 0201
C1054 1UF 20% 4V CERM-X6S 0201
C1055 1UF 20% 4V CERM-X6S 0201
C1056 1UF 20% 4V CERM-X6S 0201
C1057 1UF 20% 4V CERM-X6S 0201
C1058 1UF 20% 4V CERM-X6S 0201
C1059 1UF 20% 4V CERM-X6S 0201
C1060 1UF 20% 4V CERM-X6S 0201
C1061 1UF 20% 4V CERM-X6S 0201
C1062 1UF 20% 4V CERM-X6S 0201

NOSTUFF
C10A0 20UF 20% 2.5V X6S-CERM 0402-1
C10A1 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10A2 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10A3 20UF 20% 2.5V X6S-CERM 0402-1
C10A4 20UF 20% 2.5V X6S-CERM 0402-1
C10A5 20UF 20% 2.5V X6S-CERM 0402-1
C10A6 20UF 20% 2.5V X6S-CERM 0402-1
C10A7 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10A8 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10A9 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10B0 20UF 20% 2.5V X6S-CERM 0402-1
C10B1 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10B2 20UF 20% 2.5V X6S-CERM 0402-1
C10B3 20UF 20% 2.5V X6S-CERM 0402-1
C10B4 20UF 20% 2.5V X6S-CERM 0402-1
C10B5 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10B6 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10B7 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10B8 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10B9 20UF 20% 2.5V X6S-CERM 0402-1
C10C0 20UF 20% 2.5V X6S-CERM 0402-1
C10C1 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10C3 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10C4 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10C5 20UF 20% 2.5V X6S-CERM 0402-1
C10C6 20UF 20% 2.5V X6S-CERM 0402-1
C10C7 20UF 20% 2.5V X6S-CERM 0402-1

C10D0 20UF 20% 2.5V X6S-CERM 0402-1
C10D1 20UF 20% 2.5V X6S-CERM 0402-1
C10D2 20UF 20% 2.5V X6S-CERM 0402-1
C10D3 20UF 20% 2.5V X6S-CERM 0402-1
C10D4 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10D5 20UF 20% 2.5V X6S-CERM 0402-1
C10D6 20UF 20% 2.5V X6S-CERM 0402-1
C10D7 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10E0 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10E1 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10E2 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10E3 20UF 20% 2.5V X6S-CERM 0402-1

Noise Floor caps

C10N1 12PF 5% 25V NP0-C0G 0201
C10N2 12PF 5% 25V NP0-C0G 0201
C10N3 12PF 5% 25V NP0-C0G 0201
C10N4 12PF 5% 25V NP0-C0G 0201
C10N5 12PF 5% 25V NP0-C0G 0201
C10N6 12PF 5% 25V NP0-C0G 0201
C10N7 12PF 5% 25V NP0-C0G 0201

Place near inductors on bottom side.

NOSTUFF
C10Z1 20UF 20% 2.5V X6S-CERM 0402-1
C10Z2 20UF 20% 2.5V X6S-CERM 0402-1
C10Z3 20UF 20% 2.5V X6S-CERM 0402-1
C10Z4 20UF 20% 2.5V X6S-CERM 0402-1
C10Z5 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10Z6 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10Z7 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10Z8 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10Z9 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10ZA 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10ZB 20UF 20% 2.5V X6S-CERM 0402-1
NOSTUFF
C10ZC 20UF 20% 2.5V X6S-CERM 0402-1

C1068 220UF 20% 2V ELEC SM-COMBO
C1069 220UF 20% 2V ELEC SM-COMBO
C1070 220UF 20% 2V ELEC SM-COMBO
C1071 220UF 20% 2V ELEC SM-COMBO
C1072 220UF 20% 2V ELEC SM-COMBO
C1073 220UF 20% 2V ELEC SM-COMBO

116 109 PP1V2_S3_CPUDDR

Place on bottom side of U0500.

C1080 20UF 20% 2.5V X6S-CERM 0402-1
C1081 20UF 20% 2.5V X6S-CERM 0402-1
C1082 20UF 20% 2.5V X6S-CERM 0402-1
C1083 20UF 20% 2.5V X6S-CERM 0402-1
C1084 20UF 20% 2.5V X6S-CERM 0402-1
C1085 20UF 20% 2.5V X6S-CERM 0402-1

Place on bottom side of U0500

C1090 20UF 20% 2.5V X6S-CERM 0402-1
C1091 20UF 20% 2.5V X6S-CERM 0402-1
C1092 20UF 20% 2.5V X6S-CERM 0402-1
C1093 20UF 20% 2.5V X6S-CERM 0402-1
C1094 20UF 20% 2.5V X6S-CERM 0402-1
C1095 20UF 20% 2.5V X6S-CERM 0402-1

CPU VDDQ Decoupling

Intel recommendation: 10x 10uF 0402, 4x 22uF 0602
Apple Implementation:

CPU VCCIO Decoupling

Intel recommendation: 3x 10uF 0402 (opposite CPU)
Apple Implementation:

Place near U0500 one bottom side about U0500 side bottom side

109 PPVCCIO_S0_CPU

C1086 20UF 20% 2.5V X6S-CERM 0402-1
C1087 20UF 20% 2.5V X6S-CERM 0402-1
C1088 20UF 20% 2.5V X6S-CERM 0402-1
C1089 20UF 20% 2.5V X6S-CERM 0402-1
C108A 20UF 20% 2.5V X6S-CERM 0402-1

NOTE: Intel decoupling recommendations from CBR schematics for Skylake H doc#557227 and PDG section 48.1 (document# 546884)

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE	CPU Decoupling 1 [10]
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Vcc GT Slice Core Decoupling from 20140905 BOM

CPU VGTSlice Decoupling

Intel recommendation: 7x 220uF, 6x 47uF 0805, 6x 22uF 0603, 35x 10uF 0402, 68 1uF 0201
Apple Implementation:

Board Edge: 4x220uF, 7x 47uF rest on back side

116 109 PPVCCGT_S0_CPU

Place on bottom side of U0500

C1100 1UF 20% 4V CERM-X6S 0201
C1101 1UF 20% 4V CERM-X6S 0201
C1102 1UF 20% 4V CERM-X6S 0201
C1103 1UF 20% 4V CERM-X6S 0201
C1104 1UF 20% 4V CERM-X6S 0201
C1105 1UF 20% 4V CERM-X6S 0201
C1106 1UF 20% 4V CERM-X6S 0201
C1107 1UF 20% 4V CERM-X6S 0201
C1108 1UF 20% 4V CERM-X6S 0201
C1109 1UF 20% 4V CERM-X6S 0201
C1110 1UF 20% 4V CERM-X6S 0201
C1111 1UF 20% 4V CERM-X6S 0201
C1112 1UF 20% 4V CERM-X6S 0201
C1113 1UF 20% 4V CERM-X6S 0201
C1114 1UF 20% 4V CERM-X6S 0201
C1115 1UF 20% 4V CERM-X6S 0201
C1116 1UF 20% 4V CERM-X6S 0201
C1117 1UF 20% 4V CERM-X6S 0201
C1118 1UF 20% 4V CERM-X6S 0201
C1119 1UF 20% 4V CERM-X6S 0201
C1120 1UF 20% 4V CERM-X6S 0201
C1121 1UF 20% 4V CERM-X6S 0201
C1122 1UF 20% 4V CERM-X6S 0201
C1123 1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1124 1UF 20% 4V CERM-X6S 0201
C1125 1UF 20% 4V CERM-X6S 0201
C1126 1UF 20% 4V CERM-X6S 0201
C1127 1UF 20% 4V CERM-X6S 0201
C1128 1UF 20% 4V CERM-X6S 0201
C1129 1UF 20% 4V CERM-X6S 0201
C1130 1UF 20% 4V CERM-X6S 0201
C1131 1UF 20% 4V CERM-X6S 0201
C1132 1UF 20% 4V CERM-X6S 0201
C1133 1UF 20% 4V CERM-X6S 0201
C1134 1UF 20% 4V CERM-X6S 0201
C1135 1UF 20% 4V CERM-X6S 0201
C1136 1UF 20% 4V CERM-X6S 0201
C1137 1UF 20% 4V CERM-X6S 0201
C1138 1UF 20% 4V CERM-X6S 0201
C1139 1UF 20% 4V CERM-X6S 0201
C1140 1UF 20% 4V CERM-X6S 0201
C1141 1UF 20% 4V CERM-X6S 0201
C1142 1UF 20% 4V CERM-X6S 0201
C1143 1UF 20% 4V CERM-X6S 0201
C1144 1UF 20% 4V CERM-X6S 0201
C1145 1UF 20% 4V CERM-X6S 0201
C1146 1UF 20% 4V CERM-X6S 0201
C1147 1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1148 1UF 20% 4V CERM-X6S 0201
C1149 1UF 20% 4V CERM-X6S 0201
C1150 1UF 20% 4V CERM-X6S 0201
C1151 1UF 20% 4V CERM-X6S 0201
C1152 1UF 20% 4V CERM-X6S 0201
C1153 1UF 20% 4V CERM-X6S 0201
C1154 1UF 20% 4V CERM-X6S 0201
C1155 1UF 20% 4V CERM-X6S 0201
C1156 1UF 20% 4V CERM-X6S 0201
C1157 1UF 20% 4V CERM-X6S 0201
C1158 1UF 20% 4V CERM-X6S 0201
C1159 1UF 20% 4V CERM-X6S 0201
C1160 1UF 20% 4V CERM-X6S 0201
C1161 1UF 20% 4V CERM-X6S 0201
C1162 1UF 20% 4V CERM-X6S 0201
C1163 1UF 20% 4V CERM-X6S 0201
C1164 1UF 20% 4V CERM-X6S 0201
C1165 1UF 20% 4V CERM-X6S 0201
C1166 1UF 20% 4V CERM-X6S 0201
C1167 1UF 20% 4V CERM-X6S 0201

NOSTUFF
C11A0 20UF 20% 2.5V X6S-CERM 0402-1
C11A1 20UF 20% 2.5V X6S-CERM 0402-1
C11A2 20UF 20% 2.5V X6S-CERM 0402-1
C11A3 20UF 20% 2.5V X6S-CERM 0402-1
C11A4 20UF 20% 2.5V X6S-CERM 0402-1
C11A5 20UF 20% 2.5V X6S-CERM 0402-1
C11A6 20UF 20% 2.5V X6S-CERM 0402-1
C11A7 20UF 20% 2.5V X6S-CERM 0402-1
C11A8 20UF 20% 2.5V X6S-CERM 0402-1
C11A9 20UF 20% 2.5V X6S-CERM 0402-1
C11B0 20UF 20% 2.5V X6S-CERM 0402-1
C11B1 20UF 20% 2.5V X6S-CERM 0402-1
C11B2 20UF 20% 2.5V X6S-CERM 0402-1
C11B3 20UF 20% 2.5V X6S-CERM 0402-1
C11B4 20UF 20% 2.5V X6S-CERM 0402-1
C11B5 20UF 20% 2.5V X6S-CERM 0402-1
C11B6 20UF 20% 2.5V X6S-CERM 0402-1
C11B7 20UF 20% 2.5V X6S-CERM 0402-1
C11B8 20UF 20% 2.5V X6S-CERM 0402-1
C11B9 20UF 20% 2.5V X6S-CERM 0402-1
C11C0 20UF 20% 2.5V X6S-CERM 0402-1
C11C1 20UF 20% 2.5V X6S-CERM 0402-1
C11C2 20UF 20% 2.5V X6S-CERM 0402-1
C11C3 20UF 20% 2.5V X6S-CERM 0402-1
C11C4 20UF 20% 2.5V X6S-CERM 0402-1
C11C5 20UF 20% 2.5V X6S-CERM 0402-1
C11C6 20UF 20% 2.5V X6S-CERM 0402-1
C11C7 20UF 20% 2.5V X6S-CERM 0402-1
C11C8 20UF 20% 2.5V X6S-CERM 0402-1
C11C9 20UF 20% 2.5V X6S-CERM 0402-1
C11D0 20UF 20% 2.5V X6S-CERM 0402-1

NOSTUFF
C11F0 20UF 20% 2.5V X6S-CERM 0402-1
C11F1 20UF 20% 2.5V X6S-CERM 0402-1
C11F2 20UF 20% 2.5V X6S-CERM 0402-1
C11F3 20UF 20% 2.5V X6S-CERM 0402-1
C11F4 20UF 20% 2.5V X6S-CERM 0402-1
C11F5 20UF 20% 2.5V X6S-CERM 0402-1
C11F6 20UF 20% 2.5V X6S-CERM 0402-1
C11F7 20UF 20% 2.5V X6S-CERM 0402-1
C11E0 20UF 20% 2.5V X6S-CERM 0402-1
C11E1 20UF 20% 2.5V X6S-CERM 0402-1
C11E2 20UF 20% 2.5V X6S-CERM 0402-1
C11E3 20UF 20% 2.5V X6S-CERM 0402-1
C11E4 20UF 20% 2.5V X6S-CERM 0402-1
C11E5 20UF 20% 2.5V X6S-CERM 0402-1

NOSTUFF
C11D4 20UF 20% 2.5V X6S-CERM 0402-1
C11D3 20UF 20% 2.5V X6S-CERM 0402-1
C11D2 20UF 20% 2.5V X6S-CERM 0402-1
C11D1 20UF 20% 2.5V X6S-CERM 0402-1

C1168 220UF 20% 2V ELEC SM-COMBO
C1169 220UF 20% 2V ELEC SM-COMBO
C1170 220UF 20% 2V ELEC SM-COMBO
C1171 220UF 20% 2V ELEC SM-COMBO
C1172 220UF 20% 2V ELEC SM-COMBO

CPU VCCSTG Decoupling

110 18 8 6 PP1V0_S0SW

Place near U0500 on bottom side

C11L1 1UF 20% 4V CERM-X6S 0201
C11L2 1UF 20% 4V CERM-X6S 0201

CPU VCCPLL and VCCST Decoupling

110 8 PP1V0_S3
110 8 6 PP1V0_S3

C11M1 1UF 20% 4V CERM-X6S 0201
C11M2 1UF 20% 4V CERM-X6S 0201

Place near U0500 on bottom side

109 PPVCCSA_S0_CPU

Place on bottom side of U0500

C11H0 1UF 20% 4V CERM-X6S 0201
C11H1 1UF 20% 4V CERM-X6S 0201
C11H2 1UF 20% 4V CERM-X6S 0201

NOSTUFF
C11I0 20UF 20% 2.5V X6S-CERM 0402-1
C11I1 20UF 20% 2.5V X6S-CERM 0402-1
C11I2 20UF 20% 2.5V X6S-CERM 0402-1
C11I3 20UF 20% 2.5V X6S-CERM 0402-1
C11I4 20UF 20% 2.5V X6S-CERM 0402-1
C11I5 20UF 20% 2.5V X6S-CERM 0402-1
C11I6 20UF 20% 2.5V X6S-CERM 0402-1
C11I7 20UF 20% 2.5V X6S-CERM 0402-1

NOSTUFF
C11J0 47UF 20% 6.3V POLY-TANT 0805
C11J1 47UF 20% 6.3V POLY-TANT 0805

C11K9 220UF 20% 2V ELEC SM-COMBO

CPU VCCSA Decoupling

Intel recommendation: 2x 220uF, 1x 47uF 0805. 1x 22uF. 7x 10uF 0402, 3x 1uF 0201_
2x 220uF, 1x 22uF on board edge, everything else on back side
Apple Implementation:

NOTE: Intel decoupling recommendations from CBR schematics for Skylake H doc#557227 and PDG section 48.1 (document# 546884)

BOM_COST_GROUP=CPU & CHIPSET

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CPU Decoupling 2 [11]

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OMIT_TABLE

U1100
SKL-PCH-SFF
H65946
FCBGA
SYM 4 OF 12

SYSTEM POWER MANAGEMENT

Net	Pin	Signal
SMC_PCH_SUSACK_L	AL15	GPP_A15/SUSACK* (IPU)
PM_SYSRST_L	AJ4	SYS_RESET*
PM_PCH_SYS_PWROK	AK3	SYS_PWROK
PM_PCH_PWROK	AJ11	PCH_PWROK
PLT_RST_L	AG23	GPP_B13/PLTRST*
PM_RSMRST_L	AF12	RSMRST*
SMC_PCH_SUSWARN_L	AJ16	GPP_A13/SUSWARN* /SUSPWRDNACK
PM_PWRBTN_L	AM10	GPD3/PWRBTN*
SSD_SR_EN_L	AL12	GPD1/ACPRESENT
PM_BATLOW_L (IPU)	AM12	GPD0/BATLOW*
PM_SLP_S0_L	AM22	GPP_B12/SLP_S0*
NC_PCH_SLP_WLAN_L	AH10	GPD9/SLP_WLAN*
NC_PCH_PME_L	AG16	GPP_A11/PME*
AUD_PWR_EN	AG18	GPP_A12/BMBUSY*/ISH_GP6 /SX_EXIT_HOLDOFF*
SYSCLK_CLK32K_PCH	AL8	RTCX1
NC_PCH_CLK32K_RTCX2	AM8	RTCX2
PCH_INTRUDER_L	AJ10	INTRUDER*
PCH_SRTCRST_L	AJ8	SRTCRST*
RTC_RESET_L	AH8	RTCRST*
NC_PCH_DRAM_RESET_L	AM11	DRAM_RESET*
PM_DSW_PWRGD	AF8	(OD) DSW_PWROK
PCIE_WAKE_L	AG12	(IPD-DeepSx) WAKE*
LPC_CLKRUN_L	AK14	GPP_A8/CLKRUN*
LPC_PWRDWN_L	AM15	GPP_A14/SUS_STAT*/ESPI_RESET*
PM_CLK32K_SUSCLK_R	AH12	(IPU-RSMRST#) GPD8/SUSCLK
PM_SLP_S5_L	AG10	GPD10/SLP_S5*
PM_SLP_S4_L	AK10	GPD5/SLP_S4*
PM_SLP_S3_L	AK9	GPD4/SLP_S3*
NC_PCH_SLP_A_L	AG11	GPD6/SLP_A*
PM_SLP_SUS_L	AH13	SLP_SUS*
NC_PCH_SLP_LAN_L	AK11	SLP_LAN*
SMC_WAKE_SCI_L	AL9	GPD2/LAN_WAKE*
NC_PCH_LANPHYPC	AJ13	GPD11/LANPHYPC
BT_LOW_PWR_L	AH20	GPP_B2/VRALERT*
PCH_RCIN_L_PU	AM13	GPP_A0/RCIN*/ESPI_ALERT1*
LPC_AD_R<0>	AK12	GPP_A1/LAD0/ESPI_IO0
LPC_AD_R<1>	AK13	GPP_A2/LAD1/ESPI_IO1
LPC_AD_R<2>	AG20	GPP_A3/LAD2/ESPI_IO2
LPC_AD_R<3>	AM14	GPP_A4/LAD3/ESPI_IO3
LPC_FRAME_R_L	AL14	GPP_A5/LFRAME*/ESPI_CS0*
LPC_SERIRQ	AH14	GPP_A6/SERIRQ/ESPI_CS1*
SMC_RUNTIME_SCI_L	AJ18	GPP_A7/PIRQA*/ESPI_ALERT0*
NC_PCH_GPD7	AL11	GPD7/RSVD

RTC / ESPI/LPC

R1204 NOSTUFF 0 5% 1/20W MF 0201

R1205 100K 5% 1/20W MF 201

R1440 R1441 R1442 R1443 R1444 33 5% 1/20W MF 201

PLACE_NEAR=U1100.AL14:1.25mm

PP3V0_G3H

R1201 1M 5% 1/20W MF 201

R1202 20K 5% 1/20W MF 201

R1203 20K 5% 1/20W MF 201

C1202 1UF 10% 10V X5R 402-1

C1203 1UF 10% 10V X5R 402-1

OMIT_TABLE

U1100
SKL-PCH-SFF
H65946
FCBGA
SYM 2 OF 12

CLOCK SIGNALS

Net	Pin	Signal
PCIE_CLK100M_AP_N	J5	CLKOUT_PCIE_N0
PCIE_CLK100M_AP_P	J6	CLKOUT_PCIE_P0
NC_CLKOUT_PCIE_1_N	F2	CLKOUT_PCIE_N1
NC_CLKOUT_PCIE_1_P	F1	CLKOUT_PCIE_P1
NC_CLKOUT_PCIE_2_N	K6	CLKOUT_PCIE_N2
NC_CLKOUT_PCIE_2_P	K5	CLKOUT_PCIE_P2
PCIE_CLK100M_TBT_X_N	F3	CLKOUT_PCIE_N3
PCIE_CLK100M_TBT_X_P	F4	CLKOUT_PCIE_P3
PCIE_CLK100M_TBT_T_N	G2	CLKOUT_PCIE_N4
PCIE_CLK100M_TBT_T_P	G3	CLKOUT_PCIE_P4
PCIE_CLK100M_SSD_N	E2	CLKOUT_PCIE_N5
PCIE_CLK100M_SSD_P	E1	CLKOUT_PCIE_P5
NC_CLKOUT_PCIE_6_N	K2	CLKOUT_PCIE_N6
NC_CLKOUT_PCIE_6_P	K3	CLKOUT_PCIE_P6
EG_PEG_CLK100M_N	L1	CLKOUT_PCIE_N7
EG_PEG_CLK100M_P	L2	CLKOUT_PCIE_P7
NC_CLKOUT_PCIE_8_N	M3	CLKOUT_PCIE_N8
NC_CLKOUT_PCIE_8_P	M4	CLKOUT_PCIE_P8
NC_CLKOUT_PCIE_9_N	M2	CLKOUT_PCIE_N9
NC_CLKOUT_PCIE_9_P	M1	CLKOUT_PCIE_P9
NC_CLKOUT_PCIE_10_N	R6	CLKOUT_PCIE_N10
NC_CLKOUT_PCIE_10_P	R7	CLKOUT_PCIE_P10
NC_CLKOUT_PCIE_11_N	T6	CLKOUT_PCIE_N11
NC_CLKOUT_PCIE_11_P	T5	CLKOUT_PCIE_P11
NC_CLKOUT_PCIE_12_N	N3	CLKOUT_PCIE_N12
NC_CLKOUT_PCIE_12_P	N2	CLKOUT_PCIE_P12
NC_CLKOUT_PCIE_13_N	P5	CLKOUT_PCIE_N13
NC_CLKOUT_PCIE_13_P	P6	CLKOUT_PCIE_P13
NC_CLKOUT_PCIE_14_N	N5	CLKOUT_PCIE_N14
NC_CLKOUT_PCIE_14_P	N6	CLKOUT_PCIE_P14
NC_CLKOUT_PCIE_15_N	M6	CLKOUT_PCIE_N15
NC_CLKOUT_PCIE_15_P	M7	CLKOUT_PCIE_P15
SYSCLK_CLK24M_PCH	B4	XTAL24_IN
NC_PCH_CLK24M_XTALOUT	B3	XTAL24_OUT
PCH_DIFFCLK_BIASREF	E4	XCLK_BIASREF
LPC_CLK24M_SMC_R	AJ14	GPP_A9/CLKOUT_LPC0 /ESPI_CLK
LPC_CLK24M_DPMUX_UC_R	AH15	GPP_A10/CLKOUT_LPC1
CAMERA_PWR_EN	AL16	GPP_A16/CLKOUT_48
NC_ITPXDP_CLK100MN	L6	CLKOUT_ITPXDP_N
NC_ITPXDP_CLK100MP	L5	CLKOUT_ITPXDP_P
CPU_CLK100M_BCLK_N	J3	CLKOUT_CPUBCLK_N
CPU_CLK100M_BCLK_P	J4	CLKOUT_CPUBCLK_P
CPU_CLK24M_NSSC_CLK_N	H1	CLKOUT_CPUNSSC_N
CPU_CLK24M_NSSC_CLK_P	H2	CLKOUT_CPUNSSC_P
CPU_CLK100M_PCIBCLK_N	J1	CLKOUT_CPUPCIBCLK_N
CPU_CLK100M_PCIBCLK_P	J2	CLKOUT_CPUPCIBCLK_P

R1234 2.7K 1% 1/20W MF 201

PLACE_NEAR=U1100.E4:1.25mm

R1235 22 1% 1/20W MF 201

PLACE_NEAR=U1100.AJ14:1.4mm

PCI EXPRESS
CLOCKS & CONTROL

Net	Pin	Signal
AP_CLKREQ_L_R	AL20	GPP_B5/SRCCLKREQ0*
ENETSD_CLKREQ_L	AM19	GPP_B6/SRCCLKREQ1*
CAMERA_CLKREQ_L	AK20	GPP_B7/SRCCLKREQ2*
TBT_X_CLKREQ_L_R	AL19	GPP_B8/SRCCLKREQ3*
TBT_T_CLKREQ_L_R	AH22	GPP_B9/SRCCLKREQ4*
SSD_CLKREQ_L_R	AK22	GPP_B10/SRCCLKREQ5*
TBT_W_CLKREQ_L	AM25	GPP_H0/SRCCLKREQ6*
EG_CLKREQ_OUT_L	AH26	GPP_H1/SRCCLKREQ7*
AP_S0IX_WAKE_SEL	AL25	GPP_H2/SRCCLKREQ8*
AP_S0IX_WAKE_L	AF26	GPP_H3/SRCCLKREQ9*
TBT_X_CIO_PWR_EN	AK26	GPP_H4/SRCCLKREQ10*
TBT_T_CIO_PWR_EN	AL26	GPP_H5/SRCCLKREQ11*
TBT_W_CIO_PWR_EN	AJ27	GPP_H6/SRCCLKREQ12*
TBT_X_USB_PWR_EN	AH27	GPP_H7/SRCCLKREQ13*
TBT_T_USB_PWR_EN	AM26	GPP_H8/SRCCLKREQ14*
TBT_W_USB_PWR_EN	AK27	GPP_H9/SRCCLKREQ15*

R1238 R1239 R1240 47K 5% 1/20W MF 201

R1241 R1242 R1243 R1244 R1245 R1246 100K 5% 1/20W MF 201

PP3V3_S0

BOM_COST_GROUP=CPU & CHIPSET

PP3V3_S0

BT_LOW_PWR_L R1213 10K 5% 1/20W MF 201

PP3V3_S4

SSD_SR_EN_L R1211 100K 5% 1/20W MF 201

PP3V3_SUS

PM_SYSRST_L R1247 3.0K 5% 1/20W MF 201

PP3V3_SUS

PP3V3_S5

Net	Resistor	Value
PCIE_WAKE_L	R1248	100K
SMC_WAKE_SCI_L	R1209	100K
PM_PWRBTN_L	R1210	1K
PM_BATLOW_L	R1212	10K
SMC_RUNTIME_SCI_L	R1207	100K
LPC_CLKRUN_L	R1208	10K
PCH_RCIN_L_PU	R1251	100K

PP3V3_S0

Net	Resistor	Value
LPC_SERIRQ	R1206	10K
AUD_PWR_EN	R1214	100K
CAMERA_PWR_EN	R1215	100K
AP_S0IX_WAKE_L	R1216	100K
PM_SLP_S5_L	R1230	100K
PM_SLP_S4_L	R1231	100K
PM_SLP_S3_L	R1232	100K
PM_SLP_S0_L	R1233	100K
AP_S0IX_WAKE_SEL	R1236	100K
PM_SLP_SUS_L	R1237	100K

5% 1/20W MF 201

PAGE TITLE
PCH RTC/HDA/JTAG/SATA/CLK

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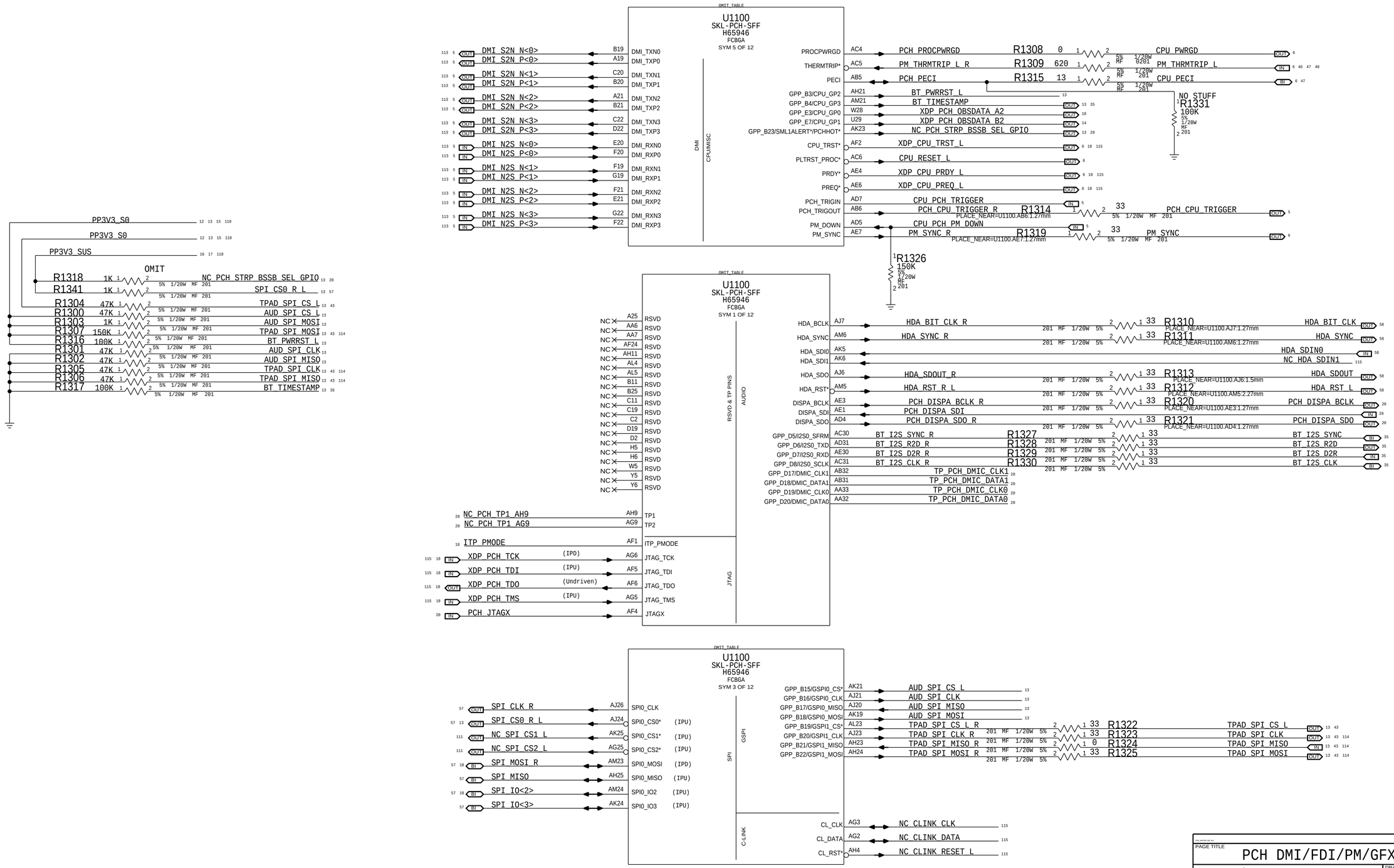

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PAGE TITLE
PCH DMI/FDI/PM/GFX/PCI

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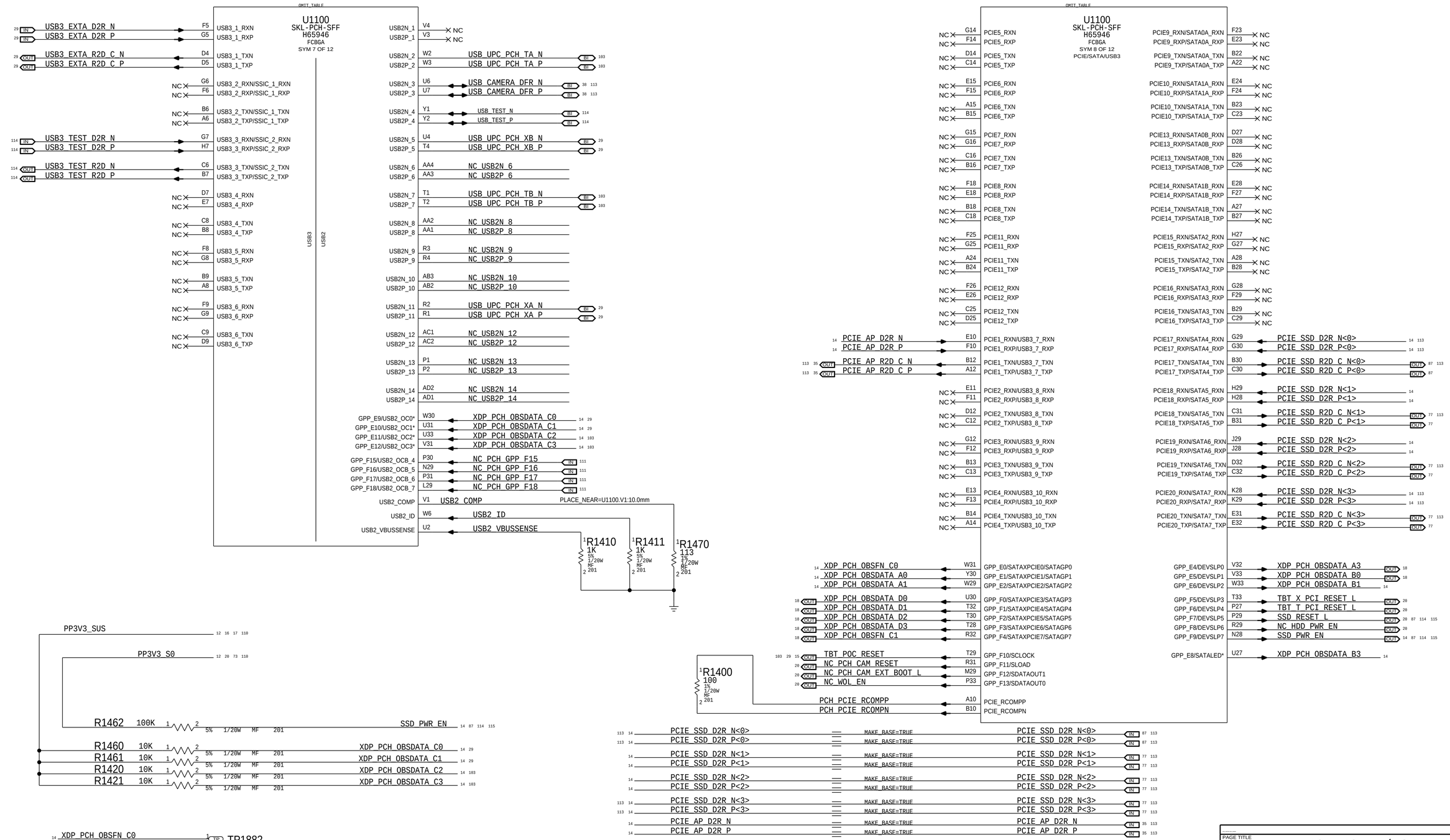

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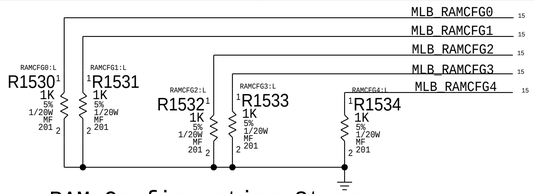
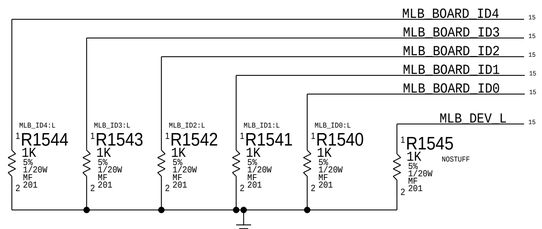


RAM Configuration Straps

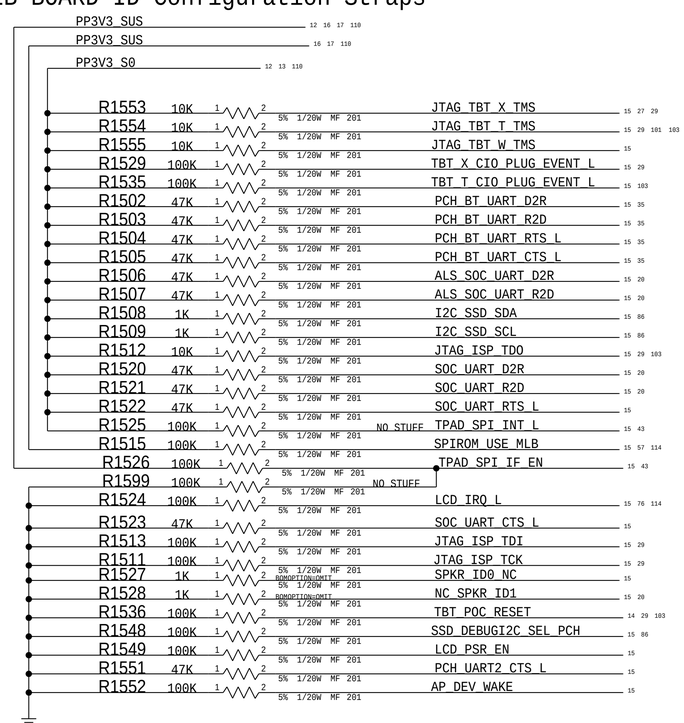
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG4:L,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L

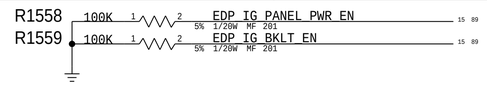
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S0006	0	RES,MF,1/20W,1KOHM,5%,0201,SMD		BOARD_ID:1F
117S0006	1	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1540	BOARD_ID:1E
117S0006	1	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1541	BOARD_ID:1D
117S0006	2	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1541,R1540	BOARD_ID:1C
117S0006	1	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1542	BOARD_ID:1B
117S0006	2	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1542,R1540	BOARD_ID:1A
117S0006	2	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1542,R1541	BOARD_ID:19
117S0006	3	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1542,R1541,R1540	BOARD_ID:18
117S0006	1	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1543	BOARD_ID:17
117S0006	2	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1543,R1540	BOARD_ID:16
117S0006	2	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1543,R1541	BOARD_ID:15
117S0006	3	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1543,R1541,R1540	BOARD_ID:14

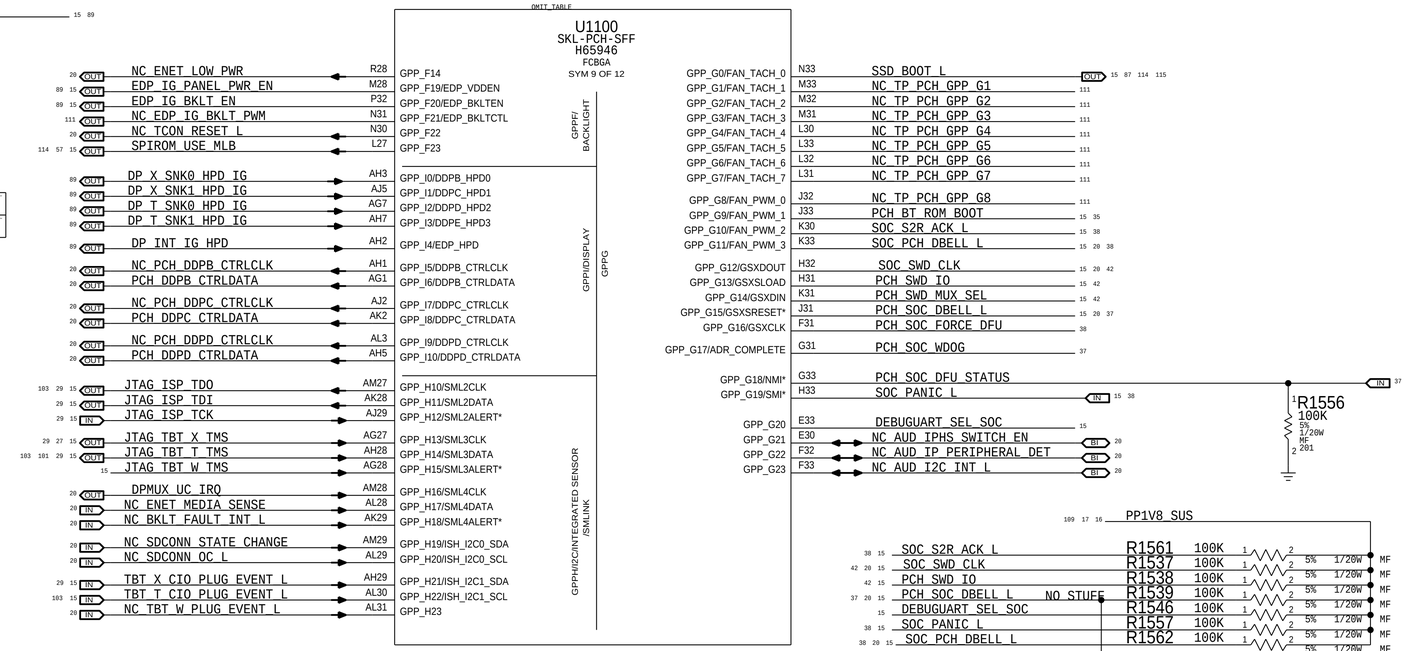
PROTO 0 = 0x1F = 1 1 1 1 1 (-01 PCB)
PROTO 0B = 0x1E = 1 1 1 1 0 (-02 PCB)
PROTO 1 = 0x1D = 1 1 1 0 1 (-03 PCB)
PROTO 2 = 0x1C = 1 1 1 0 0 (-04 & -05 PCB)
EVT1 = 0x1B = 1 1 0 1 1 (-06 PCB)
EVT2 = 0x1A = 1 1 0 1 0 (-07 PCB)
DVT = 0x19 = 1 1 0 0 1 (-08 PCB)
DVT1-1 = 0x18 = 1 1 0 0 0 (-09 PCB)
PVT = 0x17 = 1 0 1 1 1 (-10 PCB)
0x16 = 1 0 1 1 0
0x15 = 1 0 1 0 1
0x14 = 1 0 1 0 0

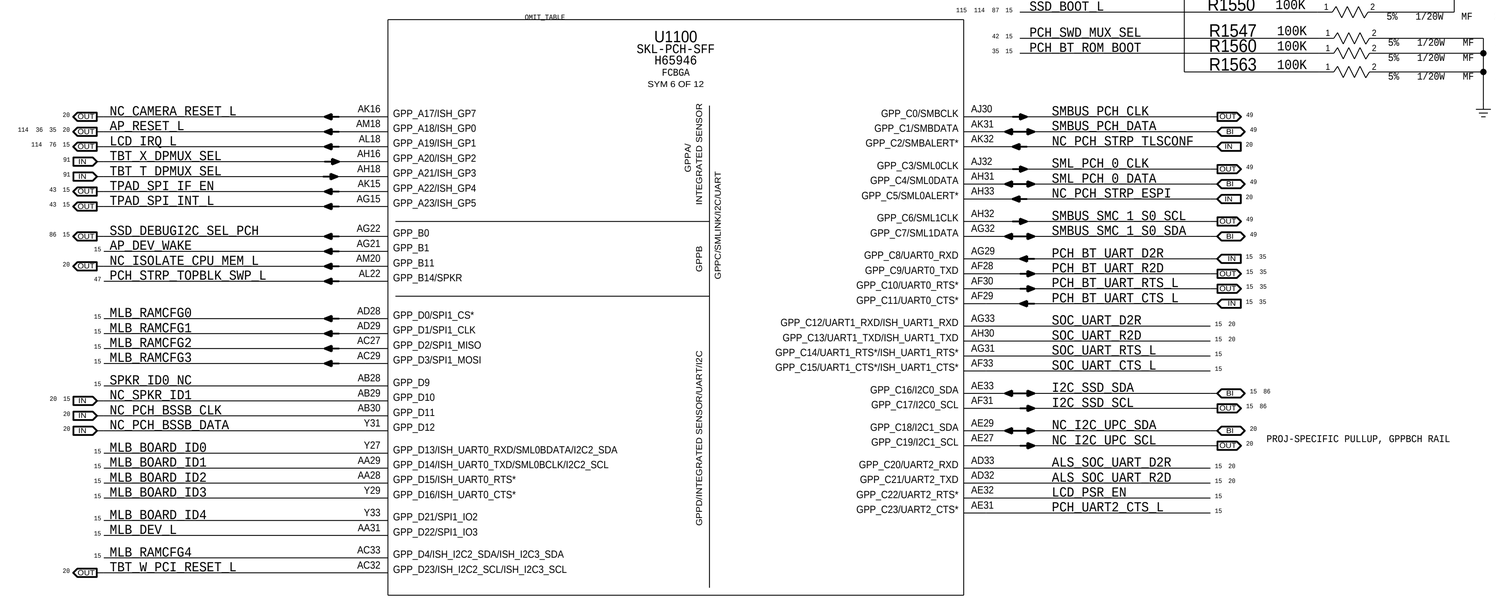


MLB BOARD ID Configuration Straps









BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
PCH GPIO/MISC/NCTF

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DRAWING NUMBER	SIZE
051-00647	D
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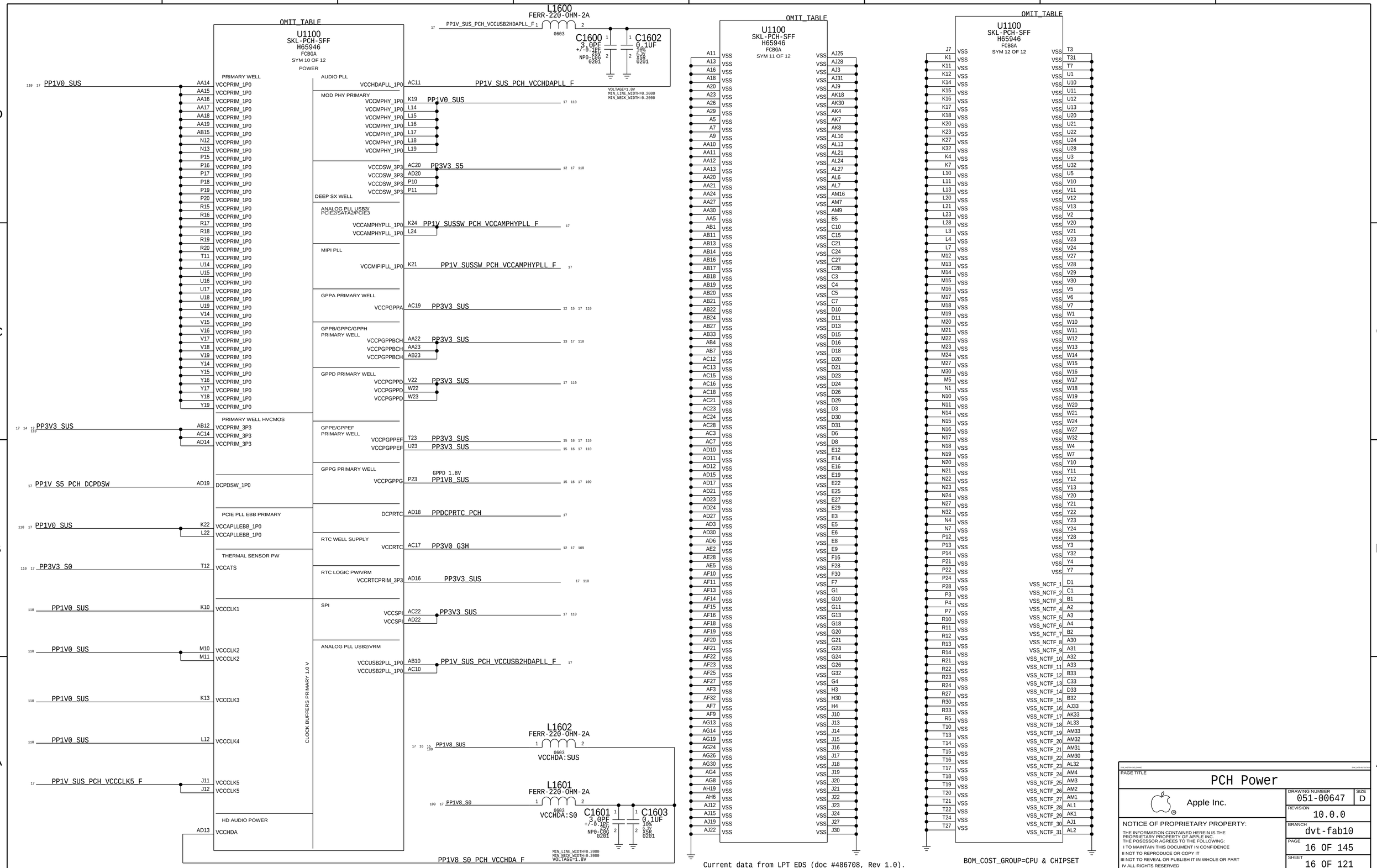
OMIT_TABLE
U1100
SKL-PCH-SFF
H65946
FCBGA
SYM 10 OF 12
POWER
PRIMARY WELL
AUDIO PLL
MOD PHY PRIMARY
DEEP SX WELL
ANALOG PLL USB3/ PCIE2/SATA2/PCIE3
MIPI PLL
GPPA PRIMARY WELL
GPPB/GPPC/GPPH PRIMARY WELL
GPPD PRIMARY WELL
PRIMARY WELL HVCMOS
GPPE/GPPEF PRIMARY WELL
GPPG PRIMARY WELL
PCIE PLL EBB PRIMARY
RTC WELL SUPPLY
THERMAL SENSOR PW
RTC LOGIC PW/VRM
SPI
ANALOG PLL USB2/VRM
CLOCK BUFFERS PRIMARY 1.0 V
HD AUDIO POWER
L1600
FERR-220-OHM-2A
0603
PP1V_SUS_PCH_VCCUSB2HDAPLL_F
C1600
3.0PF
+/-0.1PF
25V
NP0-C0G
0201
C1602
0.1UF
10%
6.3V
X5R
0201
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
PP1V0_SUS
PP3V3_S5
PP1V_SUSSW_PCH_VCCAMPHYPLL_F
PP3V3_SUS
GPPD 1.8V
PP1V8_SUS
PPDCPRTC_PCH
PP3V0_G3H
PP3V3_S0
PP1V_SUS_PCH_VCCUSB2HDAPLL_F
PP1V_SUS_PCH_VCCCLK5_F
PP1V8_S0
PP1V8_S0_PCH_VCCHDA_F
L1602
FERR-220-OHM-2A
0603
VCCHDA:SUS
L1601
FERR-220-OHM-2A
0603
VCCHDA:S0
C1601
3.0PF
+/-0.1PF
25V
NP0-C0G
0201
C1603
0.1UF
10%
6.3V
X5R
0201
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.8V
OMIT_TABLE
U1100
SKL-PCH-SFF
H65946
FCBGA
SYM 11 OF 12
OMIT_TABLE
U1100
SKL-PCH-SFF
H65946
FCBGA
SYM 12 OF 12
Current data from LPT EDS (doc #486708, Rev 1.0).
BOM_COST_GROUP=CPU & CHIPSET
PAGE TITLE
PCH Power
Apple Inc.
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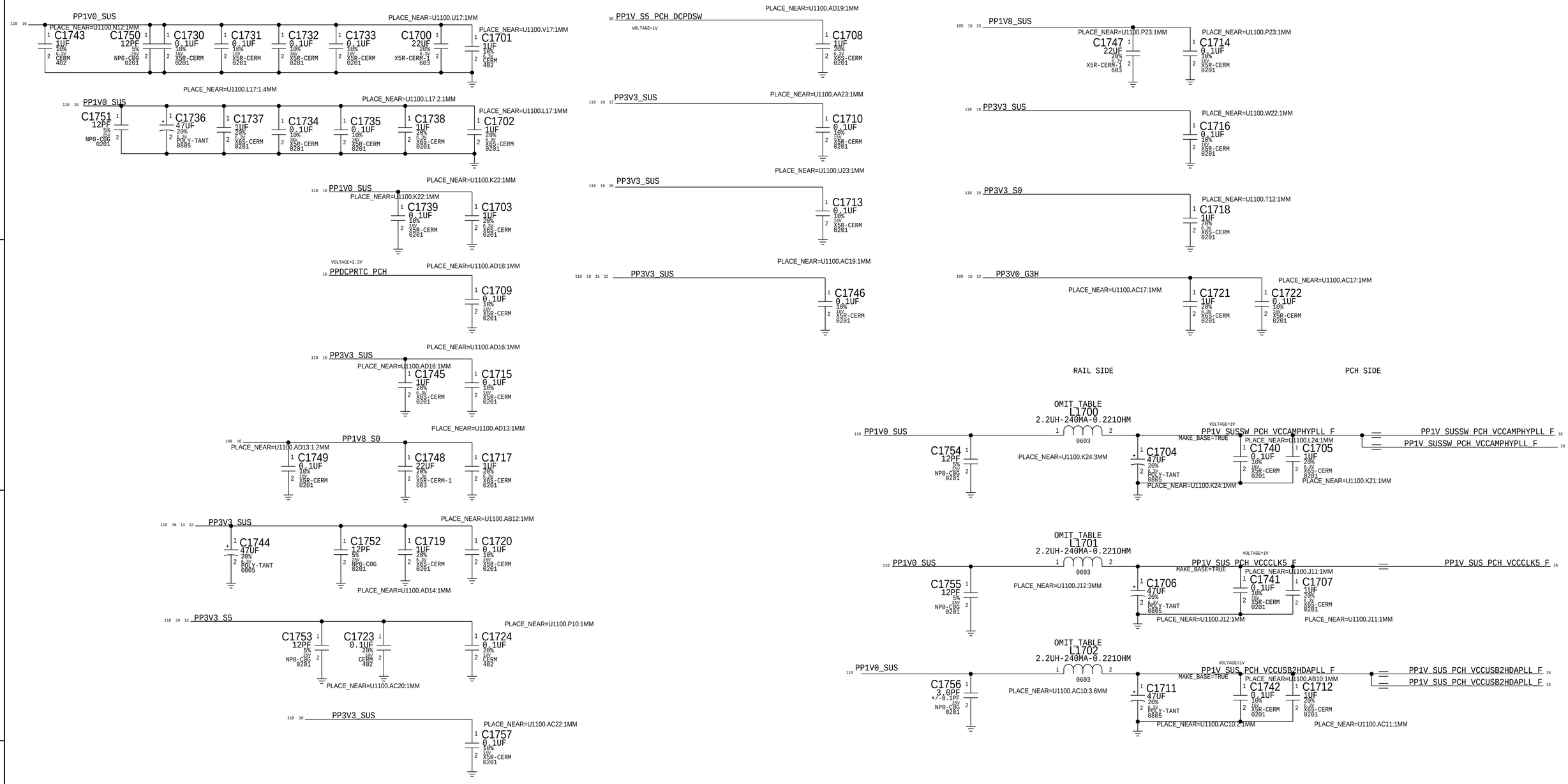
1000PF CAPS ARE INTEL PLACEHOLDERS & ALL PLACENEAR NEED TO BE UPDATED



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	3	RES,MF,1A MAX,00HM,5%,0603	L1700,L1701,L1702		

Current data from LPT EDS (doc #486708, Rev 1.0).

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
PCH DECOUPLING

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Extra BPM Testpoints

XDP_BPM_L<0> → TP1800
XDP_BPM_L<1> → TP1801
XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803

Primary / Merged (CPU/PCH) Micro2-XDP

PP1V0_SUS

PULL CFG<3> LOW WHEN XDP PRESENT
PLACE_NEAR=U0500.BN28:2.54MM
XDP:YES R1801 1K 5% 1/20W MF 201 NO_XNET_CONNECTION

XDP_CONN J1800 DF40RC-60DP-0.4V M-ST-SM1
518S0847

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

Pin	Signal	Pin	Signal
1	XDP_PIN_1	2	XDP_PRESENT_CPU
3	OBSFN_C0	4	XDP_CPU_PREQ_L
5	OBSFN_C1	6	XDP_CPU_PRDY_L
7		8	
9	OBSDATA_C0	10	CPU_CFG<0>
11	OBSDATA_C1	12	CPU_CFG<1>
13		14	
15	OBSDATA_C2	16	CPU_CFG<2>
17	OBSDATA_C3	18	CPU_CFG<3>
19		20	
21	OBSFN_D0	22	NC
23	OBSFN_D1	24	NC
25		26	
27	OBSDATA_D0	28	CPU_CFG<4>
29	OBSDATA_D1	30	CPU_CFG<5>
31		32	
33	OBSDATA_D2	34	CPU_CFG<6>
35	OBSDATA_D3	36	CPU_CFG<7>
37		38	
39	TTPCLK/HOOK4	40	HOOK0
41	TTPCLK#/HOOK5	42	HOOK1
43	VCC_OBS_CD	44	VCC_OBS_AB
45	RESET#/HOOK6	46	HOOK2
47	DBR#/HOOK7	48	HOOK3
49		50	
51	TDO	52	SDA
53	TRSTn	54	SCL
55	TDI	56	TCK1
57	TMS	58	TCK0
59	XDP_PRESENT#	60	
61		62	
63		64	

Signal	Net
CPU_CFG<17>	OBSFN_C0
CPU_CFG<16>	OBSFN_C1
CPU_CFG<8>	OBSDATA_C0
CPU_CFG<9>	OBSDATA_C1
CPU_CFG<10>	OBSDATA_C2
CPU_CFG<11>	OBSDATA_C3
CPU_CFG<19>	OBSFN_D0
CPU_CFG<18>	OBSFN_D1
CPU_CFG<12>	OBSDATA_D0
CPU_CFG<13>	OBSDATA_D1
CPU_CFG<14>	OBSDATA_D2
CPU_CFG<15>	OBSDATA_D3
NC_ITPXDP_CLK100MP	TTPCLK/HOOK4
NC_ITPXDP_CLK100MN	TTPCLK#/HOOK5
ITP_PMODE	RESET#/HOOK6
XDP_DBRESET_L	DBR#/HOOK7
XDP_PM_RSMRST_L	HOOK0
XDP_CPU_PWRBTN_L	HOOK1
SPI_MOSI_R_CONN	HOOK2
XDP_PCH_TCK	TCK1
XDP_CPU_TCK	TCK0

PP3V3_SUS
PLACE_NEAR=J1800.48:2.54MM
XDP:YES R1804 1K 5% 1/20W MF 201

PM_RSMRST_L → R1800 1K XDP:YES PLACE_NEAR=U1100.AF12:3.8MM
PM_PWRBTN_L → R1802 10 XDP:YES PLACE_NEAR=U1100.AM10:3MM
SPI_MOSI_R → R1803 1K XDP:YES PLACE_NEAR=U1100.AM23:2.54MM
XDP_CPU_TCK
PCH_JTAGX → R1835 0 XDP:YES PLACE_NEAR=J1800.58:28MM

XDP:YES C1804 0.1UF 10% 6.3V CERM-X5R 0201 PLACE_NEAR=J1800.42:28MM
XDP:YES C1800 0.1UF 10% 6.3V CERM-X5R 0201 PLACE_NEAR=J1800.44:28MM
XDP:YES C1801 0.1UF 10% 6.3V CERM-X5R 0201 PLACE_NEAR=J1800.43:28MM
XDP:YES C1806 0.1UF 10% 6.3V CERM-X5R 0201 PLACE_NEAR=J1800.47:28MM

PP1V0_S0SW

Signal	Resistor	Value	Attributes
XDP_PCH_TDO	R1890	51	XDP:YES, PLACE_NEAR=U1100.AF6:28MM
XDP_PCH_TDI	R1891	51	XDP:YES, PLACE_NEAR=U1100.AF5:28MM
XDP_PCH_TMS	R1892	51	XDP:YES, PLACE_NEAR=U1100.AG5:28MM
XDP_CPU_TDO	R1810	51	XDP:YES, PLACE_NEAR=U0500.BT28:28MM
XDP_CPU_TCK	R1813	51	XDP:YES, PLACE_NEAR=U0500.BR28:28MM
XDP_PCH_TCK	R1897	51	NOSTUFF, PLACE_NEAR=U1100.AG6:28MM
XDP_PCH_TRST_L	R1898	51	NOSTUFF, PROPER WAY TO TERMINATE?

R1830 1K 5% 1/20W MF 201 PLACE_NEAR=U0500.EB:2.54MM → ITP_PMODE

XDP:YES R1806 0 5% 1/20W MF 0201 PM_SYSRST_L

ROUTE IN STAR TOPOLOGY FROM XDP CONNECTOR.

Resistor	Value	Signal	Attributes
R1821	0	XDP_CPU_TDO	XDP:YES, PLACE_NEAR=J1800.51:2.54MM
R1822	0	XDP_CPU_TRST_L	XDP:YES, PLACE_NEAR=J1800.53:2.54MM
R1823	0	XDP_CPU_TDI	XDP:YES, PLACE_NEAR=J1800.55:2.54MM
R1824	0	XDP_CPU_TMS	XDP:YES, PLACE_NEAR=J1800.57:2.54MM

XDP_PCH_TDO
XDP_PCH_TRST_L
XDP_PCH_TDI
XDP_PCH_TMS

PP3V3_SUS → XDP:YES R1850 100K 5% 1/20W MF 201 → XDP_PRESENT_L

PP3V3_SUS → XDP:YES C1830 0.1UF 10% 10V X5R-CERM 0201

U1830 74AUP1G07GF SOT891 (VCC, A, Y, GND, NC, (OD))
XDP:YES
NC → NC

SPI_IO2_STRAP_L → R1831 1.5K 5% 1/20W MF 201 XDP:YES NO_XNET_CONNECTION → SPI_IO<2> (STRAP TO PCH)
PLACE_NEAR=U1830.4:7.54MM
PLACE_NEAR=U1830.4:2.54MM → R1832 49.9 1% 1/20W MF 201 NOSTUFF NO_XNET_CONNECTION

NEED TO CONNECT TO VCCST, *STG POWER LOGIC

PCH XDP Signals

These signals do not connect to the Primary (Merged) XDP connector in this architecture.
The PDG puts them on a secondary XDP connector that is only needed in some PCH debugging situation.
They are listed here to show their secondary XDP functions and to provide test points for signals that are not used elsewhere.

PCH/XDP Signals | Non-XDP Signals

Signal	Test Point
XDP_PCH_OBSDATA_A2	TP1870
XDP_PCH_OBSDATA_A3	TP1871
XDP_PCH_OBSDATA_B0	TP1872
XDP_PCH_OBSDATA_C0	TP1873
XDP_PCH_OBSDATA_C1	TP1874
XDP_PCH_OBSDATA_C2	TP1875
XDP_PCH_OBSDATA_C3	TP1876
XDP_PCH_OBSDATA_D0	TP1877
XDP_PCH_OBSDATA_D1	TP1878
XDP_PCH_OBSDATA_D2	TP1879
XDP_PCH_OBSDATA_D3	TP1880
XDP_PCH_OBSFN_C1	TP1881

Unused GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

BOM_COST_GROUP=DEBUG

DESIGN: X502/MLB
LAST CHANGE: Mon Jun 15 22:04:28 2015

PAGE TITLE: CPU/PCH Merged XDP

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DRAWING NUMBER: 051-00647 SIZE: D
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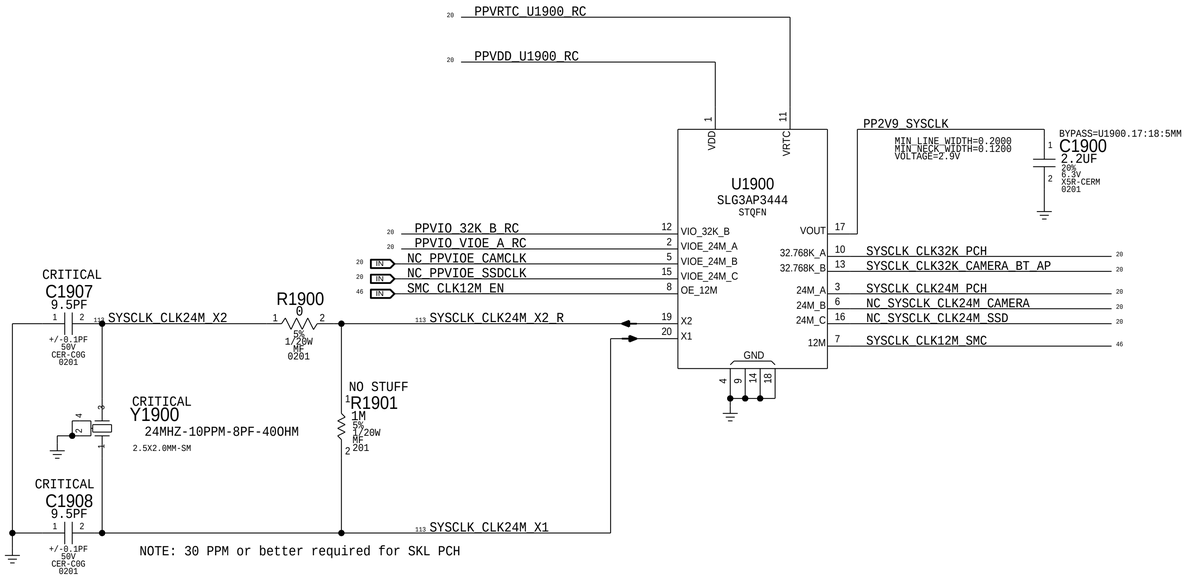
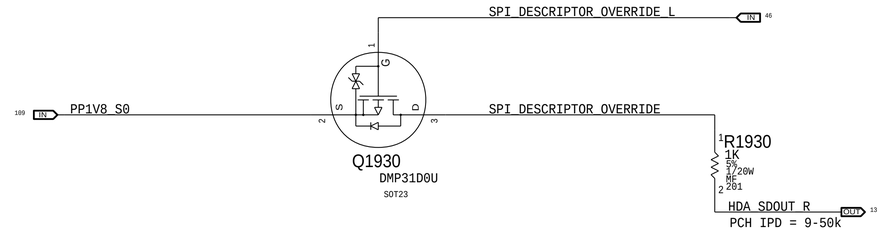
System 32kHz / 12MHz / 24MHz Clock Generator



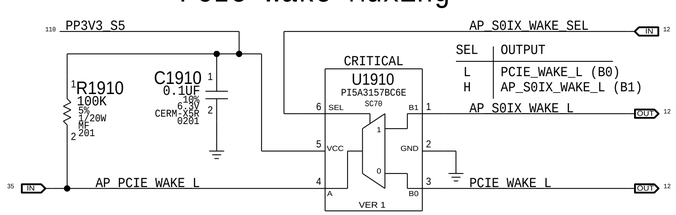
NOTE: 30 PPM or better required for SKL PCH

PCH ME Disable Strap



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
***** Circuit does not support HDA voltage >3.3V.

PCIe Wake Muxing



SEL	OUTPUT
L	PCIE_WAKE_L (B0)
H	AP_S0IX_WAKE_L (B1)

BOM_COST_GROUP=CPU & CHIPSET

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Chipset Support 1

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Platform Reset Connections

Buffered

Scrub for Layout Optimization

PP3V3_S0 — PLT_RST_L (IN) — U2071 MC74VHC1G08 SC70-HF (CRITICAL) — PLT_RST_L_BUF

C2071 0.1UF 10% 16V X5R-CERM 0201 — PLACE_NEAR=R2001:5MM

R2070 100K 5% 1/20W MF 201

R2072 4.99K 1% 1/20W MF 201 — PLACE_NEAR=U2071:5MM

NOSTUFF R2073 0 5% 1/20W MF 0201

Unbuffered

PLT_RST_L (IN)	R2000	100K	MAKE_BASE=TRUE TBT_X_PCI_RESET_L	14
	R2001	100K	TBT_X_PCI_RESET_L	27 29
	R2002	100K	MAKE_BASE=TRUE TBT_T_PCI_RESET_L	14
	R2003	10K	TBT_T_PCI_RESET_L	101
	R2004	100K	AP_RESET_L	15 35 36 114
	R2005	100K	SSD_RESET_L	14 87 114 115
			SMC_LRESET_L	46
			TBT_W_PCI_RESET_L	15

NOSTUFF

DPMUX Connections

PLT_RST_L (IN) — R2006 100K — DPMUX_LRESET_L

LPC_CLK24M_DPMUX_UC_R — R2007 22 — LPC_CLK24M_DPMUX_UC (OUT)

LPC_CLK24M_DPMUX_UC_R — MAKE_BASE=TRUE

DPMUX_UC_IRQ — MAKE_BASE=TRUE DPMUX_UC_IRQ (IN) — R2089 100K

NC_PCH_CLK24M_XTALOUT (IN) — MAKE_BASE=TRUE NC_PCH_CLK24M_XTALOUT

MAKE_BASE=TRUE SYSCLK_CLK24M_PCH (IN) — SYSCLK_CLK24M_PCH (OUT)

NC ALIASES 3

NC_AUD_IPHS_SWITCH_EN	MAKE_BASE=TRUE NC_AUD_IPHS_SWITCH_EN
NC_AUD_IP_PERIPHERAL_DET	MAKE_BASE=TRUE NC_AUD_IP_PERIPHERAL_DET
NC_AUD_I2C_INT_L	MAKE_BASE=TRUE NC_AUD_I2C_INT_L
NC_ENET_MEDIA_SENSE	MAKE_BASE=TRUE NC_ENET_MEDIA_SENSE
NC_BKLT_FAULT_INT_L	MAKE_BASE=TRUE NC_BKLT_FAULT_INT_L
NC_SDCONN_STATE_CHANGE	MAKE_BASE=TRUE NC_SDCONN_STATE_CHANGE
NC_SDCONN_OC_L	MAKE_BASE=TRUE NC_SDCONN_OC_L
NC_TBT_W_PLUG_EVENT_L	MAKE_BASE=TRUE NC_TBT_W_PLUG_EVENT_L
SOC_UART_D2R	MAKE_BASE=TRUE SOC_UART_D2R
SOC_UART_R2D	SOC_UART_R2D

INTEL SKL DEBUG

TP_PCH_DMIC_CLK1	P2MM SM PP	PP2000
TP_PCH_DMIC_DATA1	P2MM SM PP	PP2001
TP_PCH_DMIC_CLK0	P2MM SM PP	PP2002
TP_PCH_DMIC_DATA0	P2MM SM PP	PP2003

GREENCLK CLOCK OUT ALIASES

MAKE_BASE=TRUE SYSCLK_CLK32K_PCH (IN) — SYSCLK_CLK32K_PCH (OUT)

NC_PCH_CLK32K_RTCX2 — MAKE_BASE=TRUE NC_PCH_CLK32K_RTCX2 (IN)

MAKE_BASE=TRUE SYSCLK_CLK32K_CAMERA_BT_AP (IN) — R2043 0 5% 1/20W MF 0201 — SOC_PMU_CLK_32K (OUT)

SIGNAL ALIASES

BKLT_PWM_MLB2TCON	MAKE_BASE=TRUE BKLT_PWM_MLB2TCON
ALS_SOC_UART_D2R	MAKE_BASE=TRUE ALS_SOC_UART_D2R
ALS_SOC_UART_R2D	MAKE_BASE=TRUE ALS_SOC_UART_R2D
PCH_JTAGX	MAKE_BASE=TRUE PCH_JTAGX
PCH_DISPA_BCLK	MAKE_BASE=TRUE PCH_DISPA_BCLK
PCH_DISPA_SDI	MAKE_BASE=TRUE PCH_DISPA_SDI
PCH_DISPA_SDO	MAKE_BASE=TRUE PCH_DISPA_SDO

NC ALIASES

NC_PCH_DRAM_RESET_L	MAKE_BASE=TRUE NC_PCH_DRAM_RESET_L
NC_TCON_RESET_L	MAKE_BASE=TRUE NC_TCON_RESET_L
NC_SPKR_ID1	MAKE_BASE=TRUE NC_SPKR_ID1
NC_HDD_PWR_EN	MAKE_BASE=TRUE NC_HDD_PWR_EN
NC_PCH_TP1_AH9	MAKE_BASE=TRUE NC_PCH_TP1_AH9
NC_PCH_TP1_AG9	MAKE_BASE=TRUE NC_PCH_TP1_AG9
NC_PCH_BSSB_CLK	MAKE_BASE=TRUE NC_PCH_BSSB_CLK
NC_PCH_BSSB_DATA	MAKE_BASE=TRUE NC_PCH_BSSB_DATA
NC_PCH_SLP_LAN_L	MAKE_BASE=TRUE NC_PCH_SLP_LAN_L
NC_ISOLATE_CPU_MEM_L	MAKE_BASE=TRUE NC_ISOLATE_CPU_MEM_L
NC_PCH_CAM_RESET	MAKE_BASE=TRUE NC_PCH_CAM_RESET
NC_PCH_CAM_EXT_BOOT_L	MAKE_BASE=TRUE NC_PCH_CAM_EXT_BOOT_L
NC_WOL_EN	MAKE_BASE=TRUE NC_WOL_EN
NC_ENET_LOW_PWR	MAKE_BASE=TRUE NC_ENET_LOW_PWR
NC_I2C_UPC_SDA	MAKE_BASE=TRUE NC_I2C_UPC_SDA
NC_I2C_UPC_SCL	MAKE_BASE=TRUE NC_I2C_UPC_SCL
NC_SYSCLK_CLK24M_CAMERA	MAKE_BASE=TRUE NC_SYSCLK_CLK24M_CAMERA
NC_SYSCLK_CLK24M_SSD	MAKE_BASE=TRUE NC_SYSCLK_CLK24M_SSD
NC_PCH_STRP_TLSCONF	MAKE_BASE=TRUE NC_PCH_STRP_TLSCONF
NC_PCH_STRP_ESPI	MAKE_BASE=TRUE NC_PCH_STRP_ESPI
NC_PCH_STRP_BSSB_SEL_GPIO	MAKE_BASE=TRUE NC_PCH_STRP_BSSB_SEL_GPIO
LPC_CLK24M_DPMUX_UC_R	MAKE_BASE=TRUE LPC_CLK24M_DPMUX_UC_R
NC_CAMERA_RESET_L	MAKE_BASE=TRUE NC_CAMERA_RESET_L

PCIE CLKREQS

PP3V3_S0

R2080	47K	SSD_CLKREQ_L	R2084 1K	SSD_CLKREQ_L_R — MAKE_BASE=TRUE SSD_CLKREQ_L_R
R2081	47K	TBT_X_CLKREQ_L	R2085 1K	TBT_X_CLKREQ_L_R — MAKE_BASE=TRUE TBT_X_CLKREQ_L_R
R2082	47K	TBT_T_CLKREQ_L	R2086 1K	TBT_T_CLKREQ_L_R — MAKE_BASE=TRUE TBT_T_CLKREQ_L_R
R2083	47K	AP_CLKREQ_L	R2087 1K	AP_CLKREQ_L_R — MAKE_BASE=TRUE AP_CLKREQ_L_R

GreenCLK VIOEs

MAKE_BASE=TRUE NC_PPVIOE_CAMCLK — NC_PPVIOE_CAMCLK

MAKE_BASE=TRUE NC_PPVIOE_SSDCLK — NC_PPVIOE_SSDCLK

NC ALIASES 2

NC_PCH_DDPB_CTRLCLK	MAKE_BASE=TRUE NC_PCH_DDPB_CTRLCLK
NC_PCH_DDPC_CTRLCLK	MAKE_BASE=TRUE NC_PCH_DDPC_CTRLCLK
NC_PCH_DDPD_CTRLCLK	MAKE_BASE=TRUE NC_PCH_DDPD_CTRLCLK
NC_PCH_SLP_A_L	MAKE_BASE=TRUE NC_PCH_SLP_A_L
NC_PCH_LANPHYPC	MAKE_BASE=TRUE NC_PCH_LANPHYPC
NC_PCH_GPD7	MAKE_BASE=TRUE NC_PCH_GPD7
NC_CLKOUT_PCIE_13_N	MAKE_BASE=TRUE NC_CLKOUT_PCIE_13_N
NC_CLKOUT_PCIE_13_P	MAKE_BASE=TRUE NC_CLKOUT_PCIE_13_P
NC_PCH_PME_L	MAKE_BASE=TRUE NC_PCH_PME_L
SOC_PCH_DBELL_L	MAKE_BASE=TRUE SOC_PCH_DBELL_L
SOC_SWD_CLK	MAKE_BASE=TRUE SOC_SWD_CLK
PCH_SOC_DBELL_L	MAKE_BASE=TRUE PCH_SOC_DBELL_L

PP1V8_S4 (IN) — LDO — R2016 3.3 (MIN_NECK_WIDTH=0.1750, MIN_LINE_WIDTH=0.2000, VOLTAGE=1.8V) — PPVCC_RTC_OSC

C2013 1.0UF 20% 6.3V X5R 0201-1

C2014 0.1UF 10% 6.3V CERM-X5R 0201

C2015 0.01UF 10% 16V X5R-CERM 0201

Y2001 32.768KHZ-25PPM-15PF-5.5V 2.50X2.00-SM-COMBO — VCC, EN/DIS, OUT, GND — SYSCLK_CLK32K_OSC_Y1901

R2017 0 — SYSCLK_CLK32K_WIFIBT (OUT)

R2018 0 — SYSCLK_CLK32K_OSC_SOC (PLACE_NEAR=U3900.AA22:3mm) — R2026 0 — SOC_CLK_32K (OUT)

NOSTUFF

J80 & J80G Display Port DDPB, DDPC,DDPD

PP3V3_S0

PCH_DDPB_CTRLDATA	R2050	2.2K
PCH_DDPC_CTRLDATA	R2051	2.2K
PCH_DDPD_CTRLDATA	R2052	2.2K

PP1V8_S4 (IN) — LDO — R2012 3.3 (MIN_NECK_WIDTH=0.1750, MIN_LINE_WIDTH=0.2000, VOLTAGE=1.8V) — PPVIO_32K_B_RC

C2003 1.0UF 20% 6.3V X5R 0201-1

C2002 0.1UF 10% 6.3V CERM-X5R 0201

C2001 0.1UF 10% 6.3V CERM-X5R 0201

BYPASS=U1900.12:18:5MM

Power State Debug LEDs

(For development only)

PP3V3_S5

DBGLED_S5	R2090 20K	D2090 GRN-90MCD-5MA-2.85V 0402	PLACE_SIDE=BOTTOM SILK_PART=S5_ON
DBGLED_S4	R2091 20K	D2091 GRN-90MCD-5MA-2.85V 0402	PLACE_SIDE=BOTTOM SILK_PART=STBY_ON
DBGLED_S3	R2092 20K	D2092 GRN-90MCD-5MA-2.85V 0402	PLACE_SIDE=BOTTOM SILK_PART=S3_ON
DBGLED_S0I3	R2093 20K	D2093 GRN-90MCD-5MA-2.85V 0402	PLACE_SIDE=BOTTOM SILK_PART=S0I3_ON
DBGLED_S0	R2095 20K	D2095 GRN-90MCD-5MA-2.85V 0402	PLACE_SIDE=BOTTOM SILK_PART=S0_ON

DBGLED_S4_D — Q2090 DMN5L06VK-7 SOT563 VER 3

DBGLED_S3_D — Q2090 DMN5L06VK-7 SOT563 VER 3

DBGLED_S0I3_D — Q2091 DMN5L06VK-7 SOT563 VER 3

DBGLED_S0_D — Q2091 DMN5L06VK-7 SOT563 VER 3

PM_SLP_S5_L (IN)

PM_SLP_S4_L (IN)

PM_SLP_S3_L (IN)

PM_SLP_S0_L (IN)

PP1V0_SUS (IN) F = 500kHz — R2013 3.3 (MIN_NECK_WIDTH=0.1750, MIN_LINE_WIDTH=0.2000, VOLTAGE=1.0V) — PPVIO_VIOE_A_RC

C2006 1.0UF 20% 6.3V X5R 0201-1

C2004 0.1UF 10% 6.3V CERM-X5R 0201

C2000 0.1UF 10% 6.3V CERM-X5R 0201

BYPASS=U1900.02:18:5MM

RC Filter -3dB @ 240KHz

PP3V3_G3H (IN) F = 1.7MHz — R2014 3.3 (MIN_NECK_WIDTH=0.1750, MIN_LINE_WIDTH=0.2000, VOLTAGE=3.3V) — PPVDD_U1900_RC

C2009 1.0UF 20% 6.3V X5R 0201-1

C2011 0.1UF 10% 6.3V CERM-X5R 0201

C2005 0.1UF 10% 6.3V X5R 0201

PP3V3_G3H (IN) F = 1.7MHz — R2015 3.3 (MIN_NECK_WIDTH=0.1750, MIN_LINE_WIDTH=0.2000, VOLTAGE=3.3V) — PPVRTC_U1900_RC

C2010 1.0UF 20% 6.3V X5R 0201-1

C2007 0.1UF 10% 6.3V CERM-X5R 0201

C2008 0.1UF 10% 6.3V X5R 0201

UNUSED NETS in J80

ENETSD_CLKREQ_L	OUT
CAMERA_CLKREQ_L	OUT
TBT_W_CLKREQ_L	OUT
TBT_W_CIO_PWR_EN	IN
TBT_W_USB_PWR_EN	IN

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE	Chipset Support 2
Apple Inc.	
DRAWING NUMBER	051-00647
SIZE	D
REVISION	10.0.0
BRANCH	dvt-fab10
PAGE	20 OF 145
SHEET	20 OF 121

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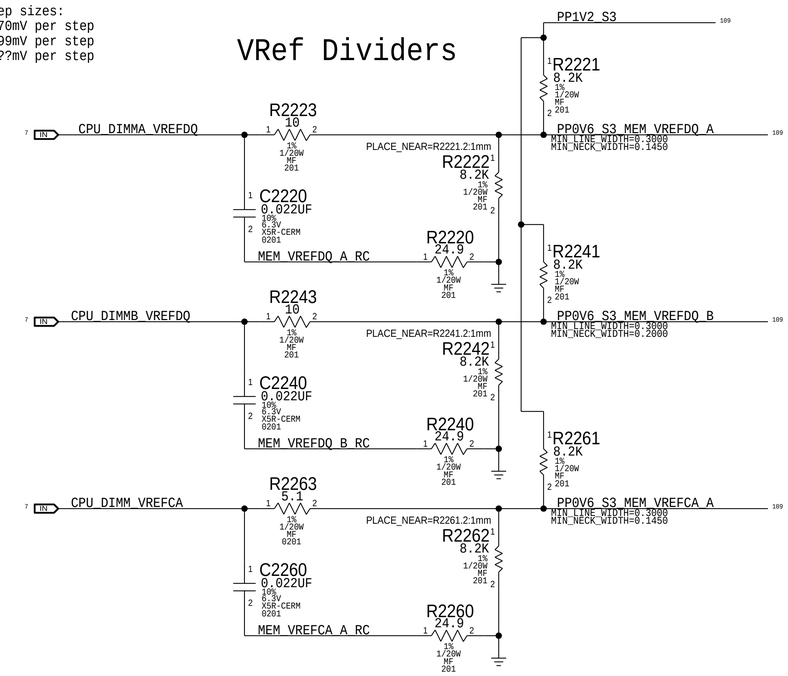
CPU-Based Margining

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step

VRef Dividers



BOM_COST_GROUP=DRAM

SYNC_MASTER=J80_MLB	SYNC_DATE=11/06/2015
PAGE TITLE: LPDDR3 VREF MARGINING	
Apple Inc.	DRAWING NUMBER: 051-00647 SIZE: D
	REVISION: 10.0.0
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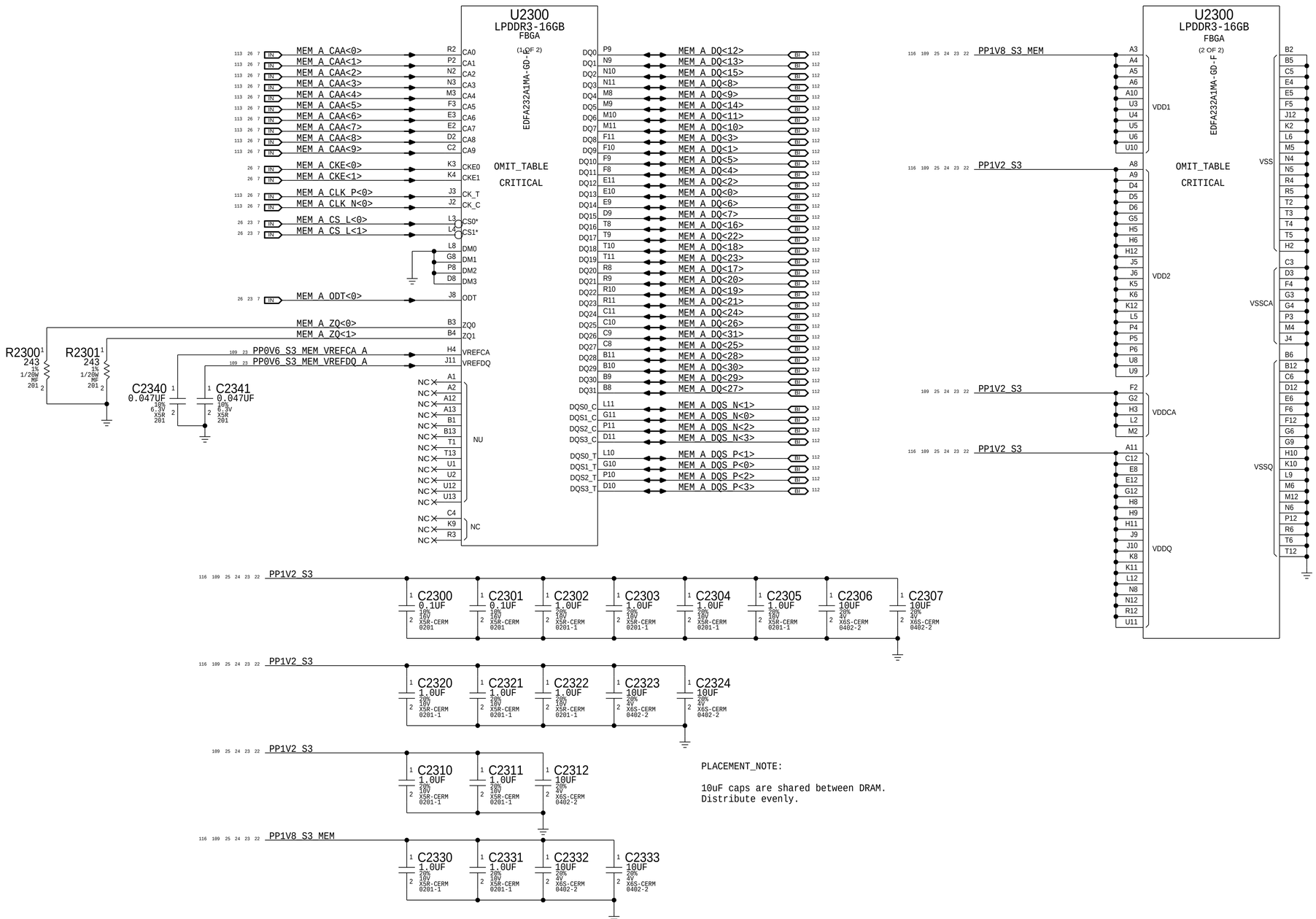
LPDDR3 CHANNEL A (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE
LPDDR3 DRAM Channel A (0-31)

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

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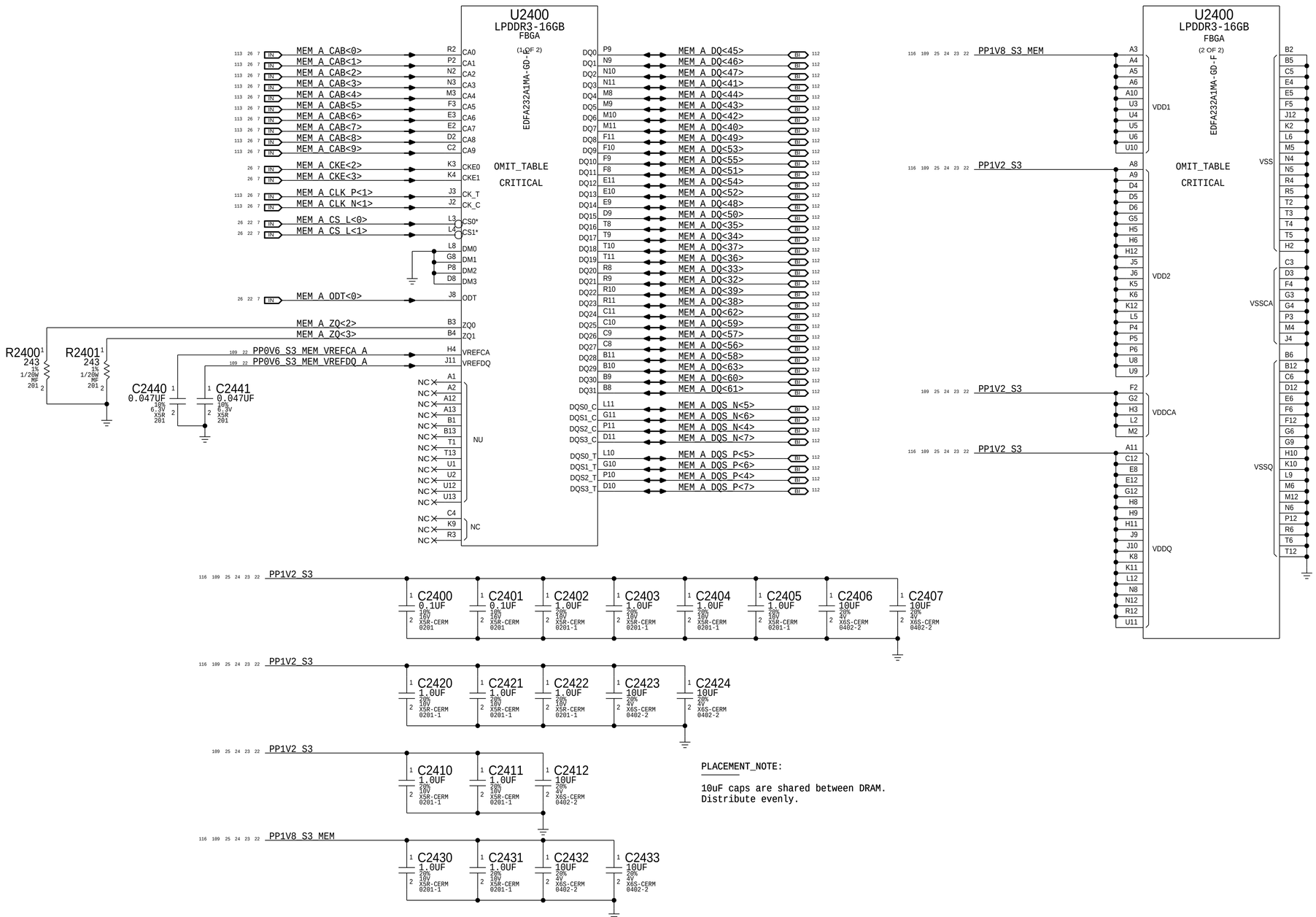
LPDDR3 CHANNEL A (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE
LPDDR3 DRAM Channel A (32-63)

Apple Inc.

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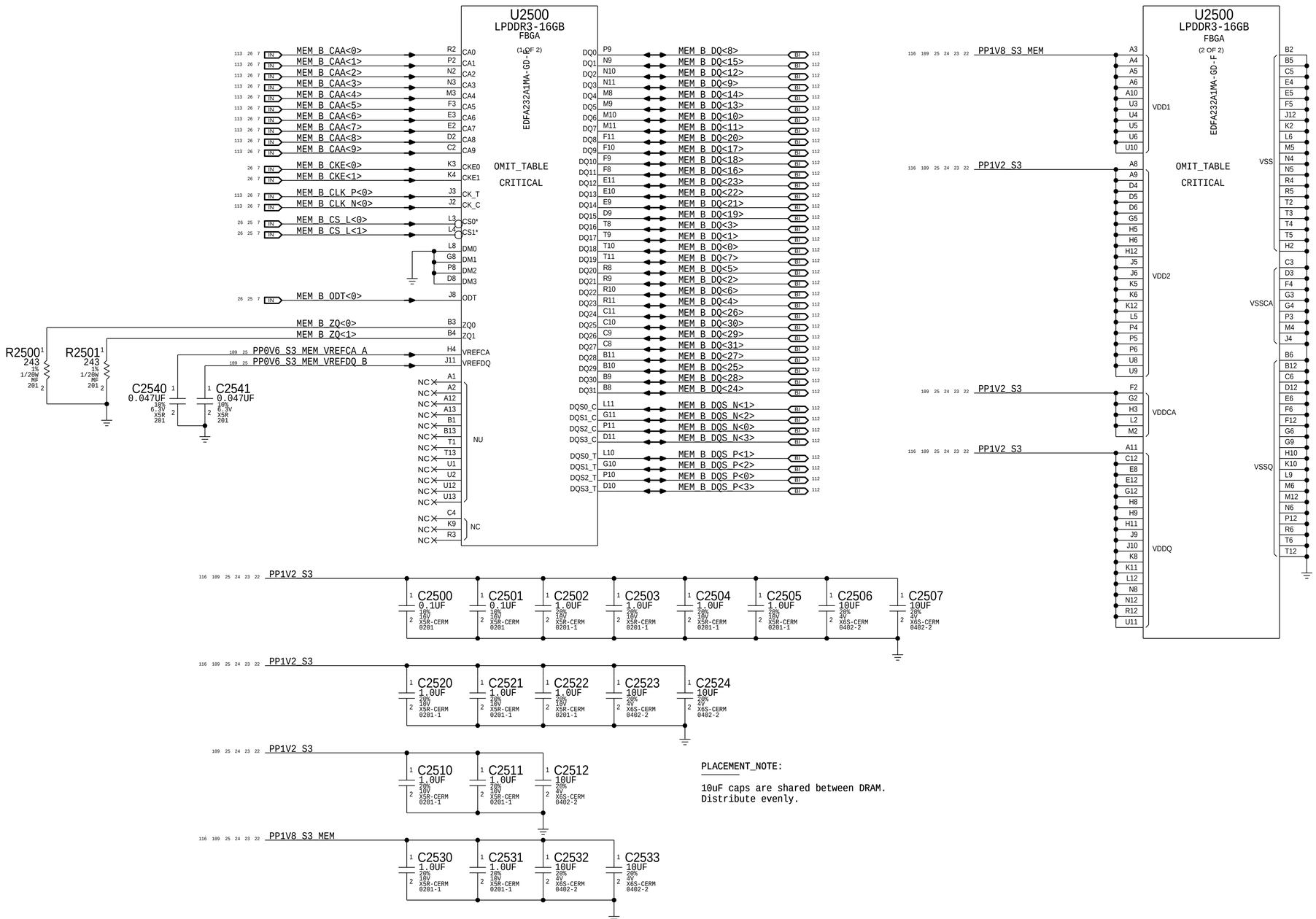
LPDDR3 CHANNEL B (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE
LPDDR3 DRAM Channel B (0-31)

Apple Inc.

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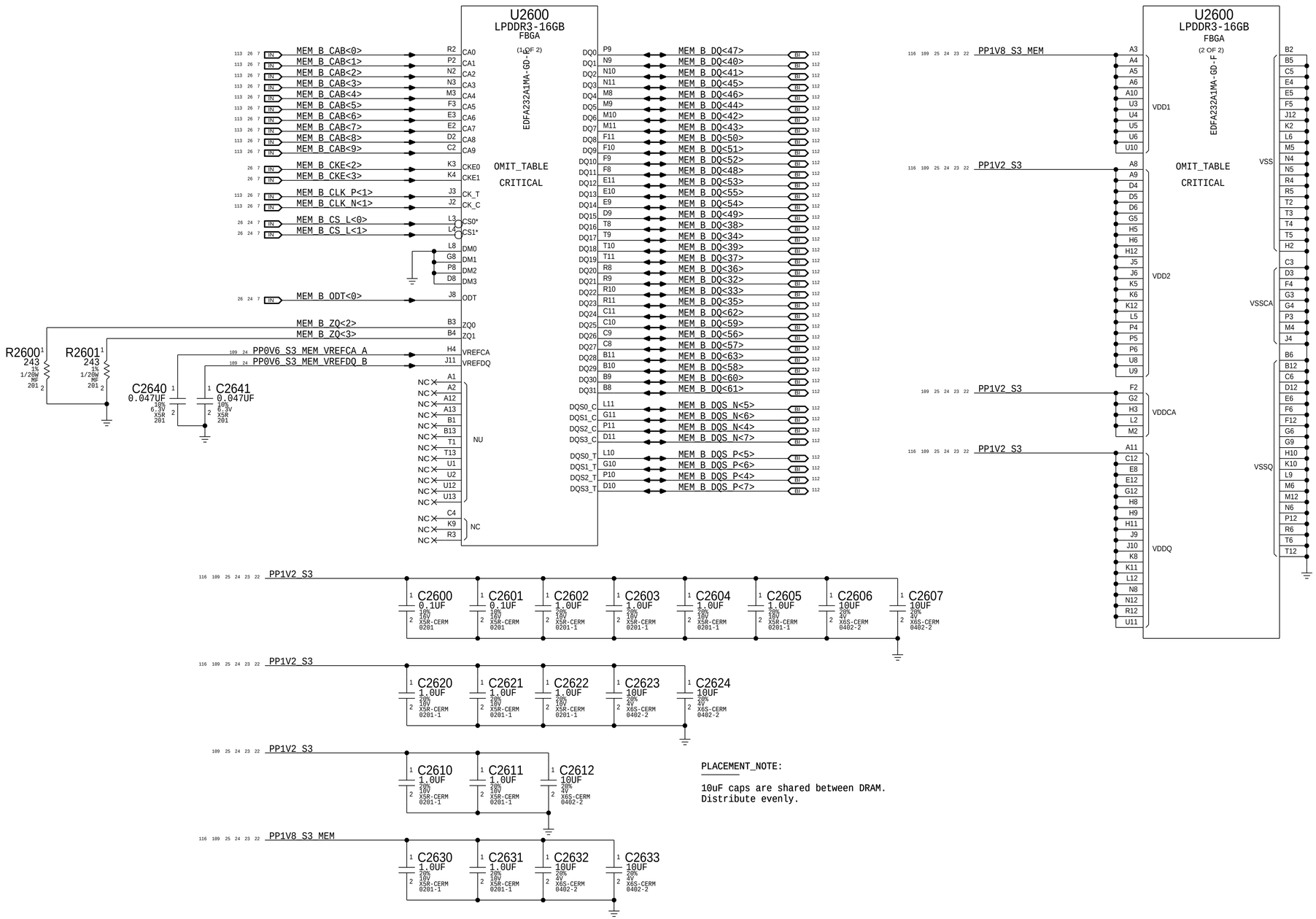
LPDDR3 CHANNEL B (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE
LPDDR3 DRAM Channel B (32-63)

Apple Inc.

DRAWING NUMBER	051-00647
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Intel recommends 68 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK

PP0V6_S0_DDRVTT

MEM_A_CAA<9>	R2700	68	1%	1/20W	201	MF	
MEM_A_CAA<8>	R2701	68	1%	1/20W	201	MF	
MEM_A_CAA<6>	R2702	68	1%	1/20W	201	MF	
MEM_A_CAA<7>	R2703	68	1%	1/20W	201	MF	
MEM_A_CAA<5>	R2704	68	1%	1/20W	201	MF	
MEM_A_CLK_P<0>	R2705	39	1%	1/20W	201	MF	
MEM_A_CLK_N<0>	R2706	39	1%	1/20W	201	MF	
MEM_A_CKE<1>	R2707	82	1%	1/20W	201	MF	
MEM_A_CKE<0>	R2708	82	1%	1/20W	201	MF	
MEM_A_CAA<4>	R2709	68	1%	1/20W	201	MF	
MEM_A_CAA<3>	R2710	68	1%	1/20W	201	MF	
MEM_A_CAA<2>	R2711	68	1%	1/20W	201	MF	
MEM_A_CAA<1>	R2712	68	1%	1/20W	201	MF	
MEM_A_CAA<0>	R2713	68	1%	1/20W	201	MF	
MEM_A_CAB<9>	R2714	68	1%	1/20W	201	MF	
MEM_A_CAB<8>	R2715	68	1%	1/20W	201	MF	
MEM_A_CAB<6>	R2716	68	1%	1/20W	201	MF	
MEM_A_CAB<7>	R2717	68	1%	1/20W	201	MF	
MEM_A_CAB<5>	R2718	68	1%	1/20W	201	MF	
MEM_A_CLK_P<1>	R2719	39	1%	1/20W	201	MF	
MEM_A_CLK_N<1>	R2720	39	1%	1/20W	201	MF	
MEM_A_CKE<2>	R2721	82	1%	1/20W	201	MF	
MEM_A_CKE<3>	R2722	82	1%	1/20W	201	MF	
MEM_A_CAB<4>	R2723	68	1%	1/20W	201	MF	
MEM_A_CAB<2>	R2724	68	1%	1/20W	201	MF	
MEM_A_CAB<3>	R2725	68	1%	1/20W	201	MF	
MEM_A_CAB<1>	R2726	68	1%	1/20W	201	MF	
MEM_A_CAB<0>	R2727	68	1%	1/20W	201	MF	
MEM_A_CS_L<0>	R2728	82	1%	1/20W	201	MF	
MEM_A_CS_L<1>	R2729	82	1%	1/20W	201	MF	
MEM_A_ODT<0>	R2730	82	1%	1/20W	201	MF	

C2700 0.47UF 20% 4V CERM-X5R-1 201
C2701 0.47UF 20% 4V CERM-X5R-1 201
C2702 0.47UF 20% 4V CERM-X5R-1 201
C2703 0.47UF 20% 4V CERM-X5R-1 201
C2704 0.47UF 20% 4V CERM-X5R-1 201
C2705 0.47UF 20% 4V CERM-X5R-1 201
C2706 0.47UF 20% 4V CERM-X5R-1 201
C2707 0.47UF 20% 4V CERM-X5R-1 201
C2708 0.47UF 20% 4V CERM-X5R-1 201
C2709 0.47UF 20% 4V CERM-X5R-1 201
C2721 12PF 5% 25V NP0-C0G 0201
CRITICAL
C2720 22UF 20% 6.3V X5R-CERM-1 603

PP0V6_S0_DDRVTT

MEM_B_CAA<9>	R2740	68	1%	1/20W	201	MF	
MEM_B_CAA<8>	R2741	68	1%	1/20W	201	MF	
MEM_B_CAA<7>	R2742	68	1%	1/20W	201	MF	
MEM_B_CAA<6>	R2743	68	1%	1/20W	201	MF	
MEM_B_CAA<5>	R2744	68	1%	1/20W	201	MF	
MEM_B_CLK_P<0>	R2745	39	1%	1/20W	201	MF	
MEM_B_CLK_N<0>	R2746	39	1%	1/20W	201	MF	
MEM_B_CKE<1>	R2747	82	1%	1/20W	201	MF	
MEM_B_CKE<0>	R2748	82	1%	1/20W	201	MF	
MEM_B_CAA<4>	R2749	68	1%	1/20W	201	MF	
MEM_B_CAA<2>	R2750	68	1%	1/20W	201	MF	
MEM_B_CAA<3>	R2751	68	1%	1/20W	201	MF	
MEM_B_CAA<1>	R2752	68	1%	1/20W	201	MF	
MEM_B_CAA<0>	R2753	68	1%	1/20W	201	MF	
MEM_B_CAB<9>	R2754	68	1%	1/20W	201	MF	
MEM_B_CAB<8>	R2755	68	1%	1/20W	201	MF	
MEM_B_CAB<7>	R2756	68	1%	1/20W	201	MF	
MEM_B_CAB<6>	R2757	68	1%	1/20W	201	MF	
MEM_B_CAB<5>	R2758	68	1%	1/20W	201	MF	
MEM_B_CLK_N<1>	R2759	39	1%	1/20W	201	MF	
MEM_B_CLK_P<1>	R2760	39	1%	1/20W	201	MF	
MEM_B_CKE<2>	R2761	82	1%	1/20W	201	MF	
MEM_B_CKE<3>	R2762	82	1%	1/20W	201	MF	
MEM_B_CAB<4>	R2763	68	1%	1/20W	201	MF	
MEM_B_CAB<2>	R2764	68	1%	1/20W	201	MF	
MEM_B_CAB<3>	R2765	68	1%	1/20W	201	MF	
MEM_B_CAB<1>	R2766	68	1%	1/20W	201	MF	
MEM_B_CAB<0>	R2767	68	1%	1/20W	201	MF	
MEM_B_CS_L<0>	R2768	82	1%	1/20W	201	MF	
MEM_B_CS_L<1>	R2769	82	1%	1/20W	201	MF	
MEM_B_ODT<0>	R2770	82	1%	1/20W	201	MF	

C2710 0.47UF 20% 4V CERM-X5R-1 201
C2711 0.47UF 20% 4V CERM-X5R-1 201
C2712 0.47UF 20% 4V CERM-X5R-1 201
C2713 0.47UF 20% 4V CERM-X5R-1 201
C2714 0.47UF 20% 4V CERM-X5R-1 201
C2715 0.47UF 20% 4V CERM-X5R-1 201
C2716 0.47UF 20% 4V CERM-X5R-1 201
C2717 0.47UF 20% 4V CERM-X5R-1 201
C2718 0.47UF 20% 4V CERM-X5R-1 201
C2719 0.47UF 20% 4V CERM-X5R-1 201
C2741 12PF 5% 25V NP0-C0G 0201
CRITICAL
C2740 22UF 20% 6.3V X5R-CERM-1 603

BOM_COST_GROUP=DRAM

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE
LPDDR3 DRAM Termination

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
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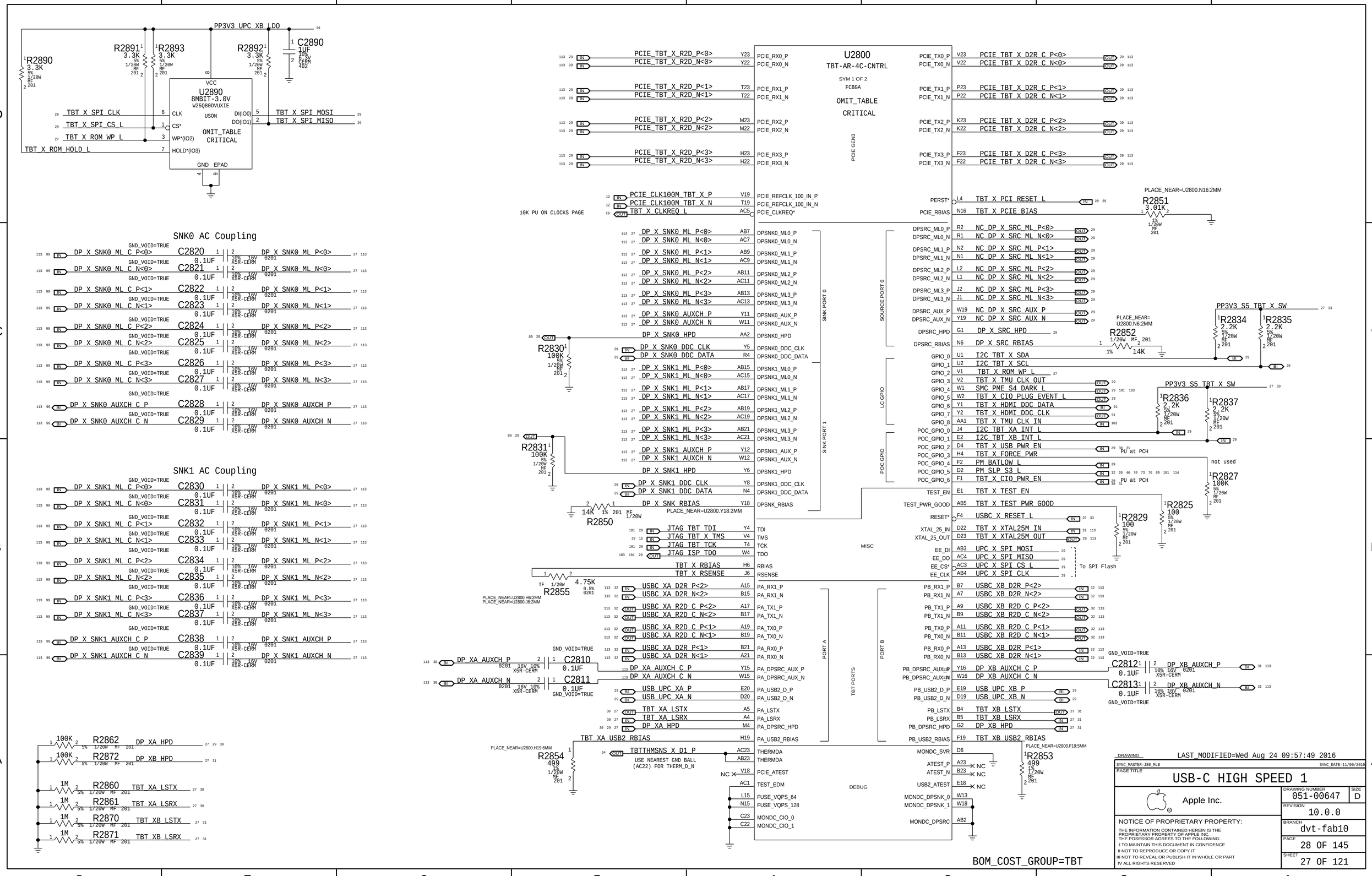
PP3V3_UPC_XB_LDO
R2890 3.3K 5% 1/20W MF 201
R2891 3.3K 5% 1/20W MF 201
R2893 3.3K 5% 1/20W MF 201
R2892 3.3K 5% 1/20W MF 201
C2890 1UF 10% 6.3V X5R-CERM 402
U2890 8MBIT-3.0V W25Q80DVUXIE USON
OMIT_TABLE CRITICAL
TBT_X_SPI_CLK
TBT_X_SPI_CS_L
TBT_X_ROM_WP_L
TBT_X_ROM_HOLD_L
TBT_X_SPI_MOSI
TBT_X_SPI_MISO
SNK0 AC Coupling
SNK1 AC Coupling
U2800 TBT-AR-4C-CNTRL
SYM 1 OF 2 FCBGA
OMIT_TABLE CRITICAL
PCIE GEN3
10K PU ON CLOCKS PAGE
PLACE_NEAR=U2800.N16:2MM
R2851 3.01K 1% 1/20W MF 201
PLACE_NEAR= U2800.N6:2MM
R2852 1/20W MF 201 1% 14K
R2830 100K 5% 1/20W MF 201
R2831 100K 5% 1/20W MF 201
R2850 14K 1% 201 MF 1/20W
PLACE_NEAR=U2800.Y18:2MM
R2855 4.75K 0.5% 0201
PLACE_NEAR=U2800.H6:2MM
PLACE_NEAR=U2800.J6:2MM
R2854 499 1% 1/20W MF 201
USE NEAREST GND BALL (AC22) FOR THERM_D_N
R2853 499 1% 1/20W MF 201
PLACE_NEAR=U2800.F19:5MM
R2834 2.2K 5% 1/20W MF 201
R2835 2.2K 5% 1/20W MF 201
R2836 2.2K 5% 1/20W MF 201
R2837 2.2K 5% 1/20W MF 201
R2827 100K 5% 1/20W MF 201
R2825 100 5% 1/20W MF 201
R2829 100 5% 1/20W MF 201
To SPI Flash
PU at PCH
not used
R2862 DP_XA_HPD
R2872 DP_XB_HPD
R2860 TBT_XA_LSTX
R2861 TBT_XA_LSRX
R2870 TBT_XB_LSTX
R2871 TBT_XB_LSRX
BOM_COST_GROUP=TBT
DRAWING LAST_MODIFIED=Wed Aug 24 09:57:49 2016
SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015
PAGE TITLE
USB-C HIGH SPEED 1
Apple Inc.
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 28 OF 145
SHEET 27 OF 121
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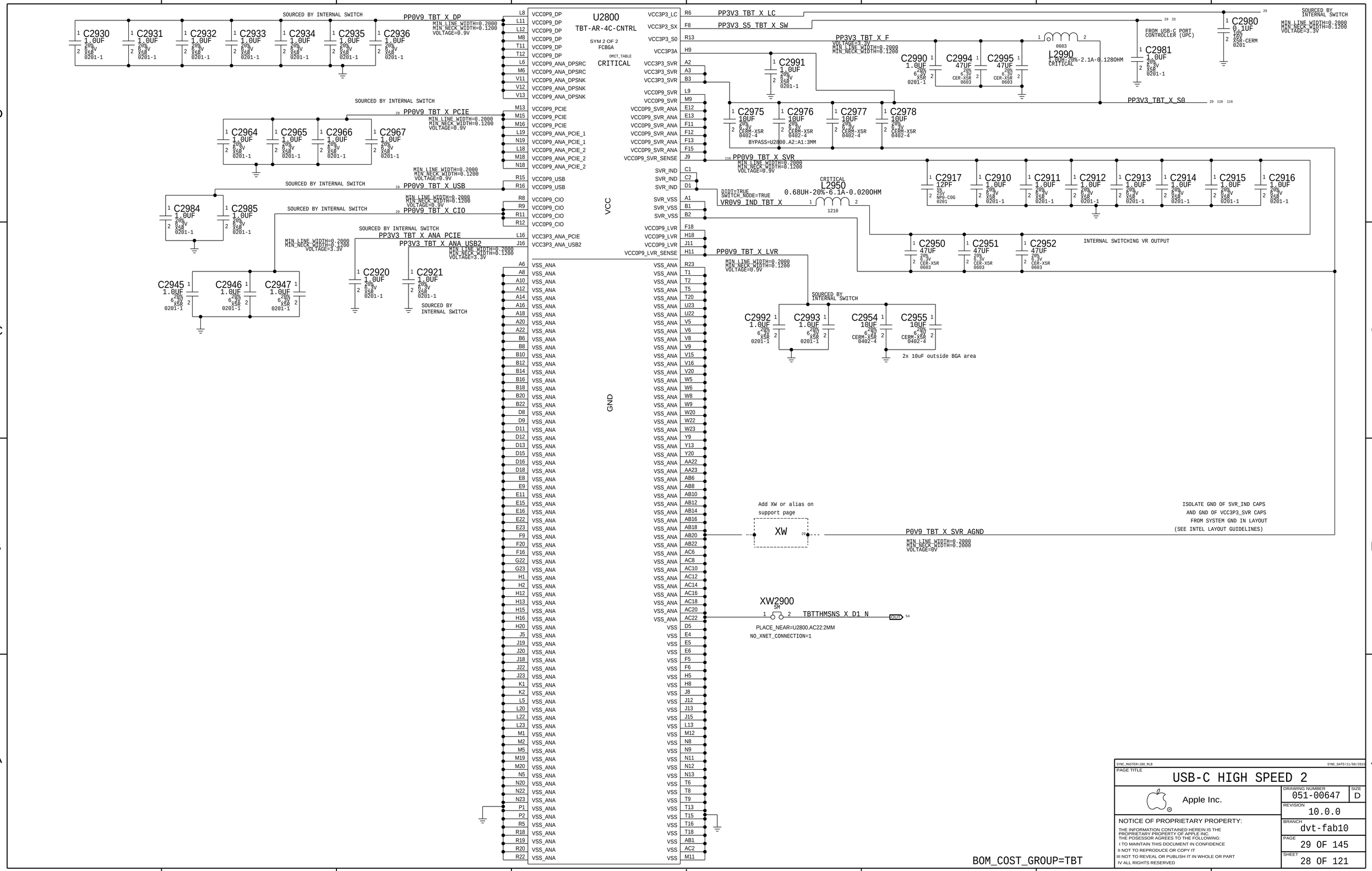

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE

USB-C HIGH SPEED 2

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

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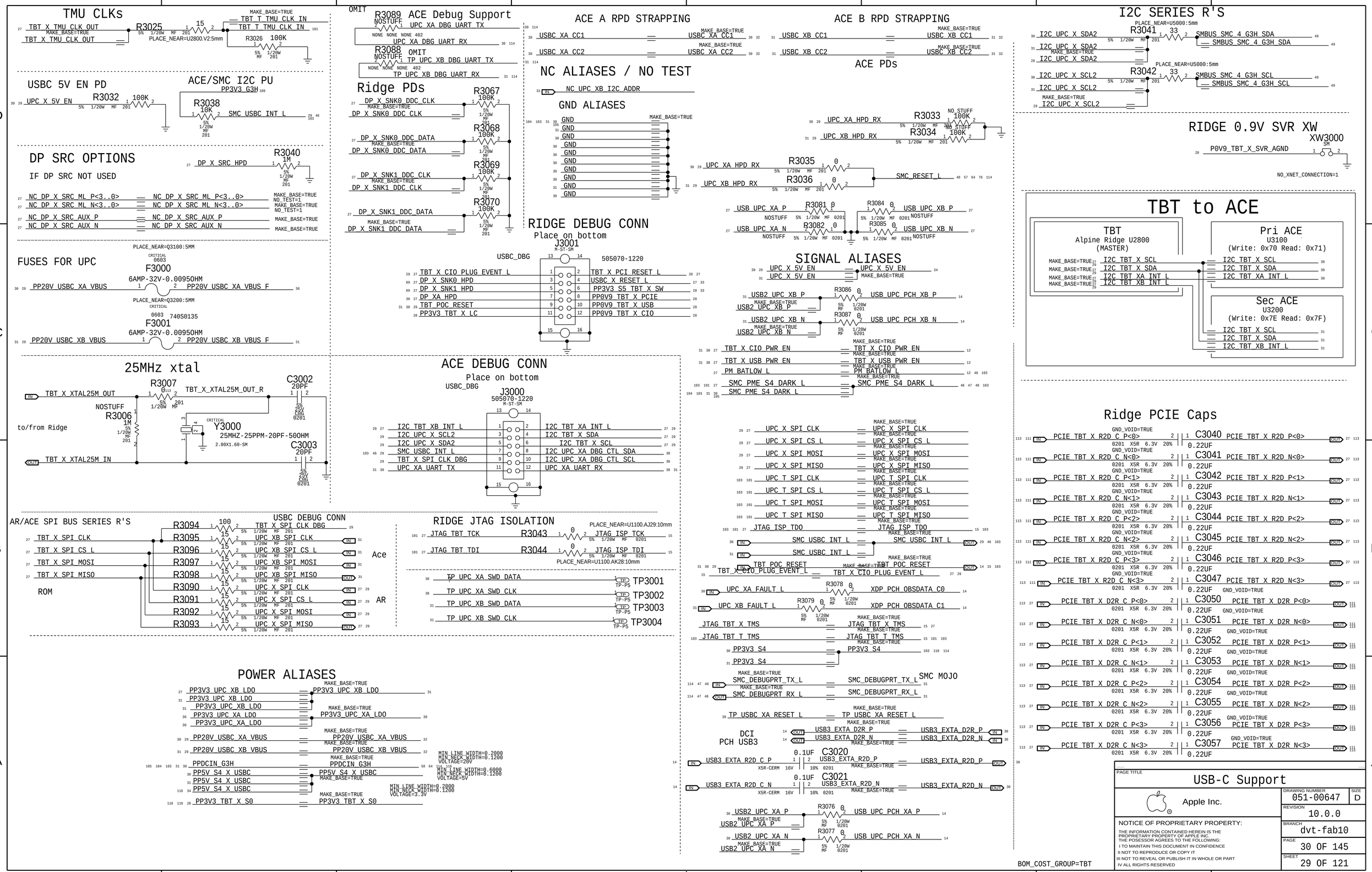
TMU CLKs
TBT_T_TMU_CLK_OUT
TBT_T_TMU_CLK_IN
R3025 15
R3026 100K
USBC 5V EN PD
UPC_X_5V_EN
R3032 100K
ACE/SMC I2C PU
PP3V3_G3H
R3038 10K
SMC_USBC_INT_L
DP SRC OPTIONS
IF DP SRC NOT USED
DP_X_SRC_HPD
R3040 1M
NC_DP_X_SRC_ML_P<3..0>
NC_DP_X_SRC_ML_N<3..0>
NC_DP_X_SRC_AUX_P
NC_DP_X_SRC_AUX_N
FUSES FOR UPC
F3000
6AMP-32V-0.0095OHM
PP20V_USBC_XA_VBUS
PP20V_USBC_XA_VBUS_F
F3001
PP20V_USBC_XB_VBUS
PP20V_USBC_XB_VBUS_F
25MHz xtal
TBT_X_XTAL25M_OUT
TBT_X_XTAL25M_OUT_R
R3007 0
C3002 20PF
R3006 1M
Y3000
25MHZ-25PPM-20PF-500HM
C3003 20PF
TBT_X_XTAL25M_IN
to/from Ridge
AR/ACE SPI BUS SERIES R'S
TBT_X_SPI_CLK
TBT_X_SPI_CS_L
TBT_X_SPI_MOSI
TBT_X_SPI_MISO
ROM
R3094 100
R3095 15
R3096 15
R3097 15
R3098 15
R3090 15
R3091 15
R3092 15
R3093 15
TBT_X_SPI_CLK_DBG
UPC_XB_SPI_CS_L
UPC_XB_SPI_MOSI
UPC_XB_SPI_MISO
UPC_X_SPI_CLK
UPC_X_SPI_CS_L
UPC_X_SPI_MOSI
UPC_X_SPI_MISO
Ace
AR
USBC DEBUG CONN
OMIT
R3089 NOSTUFF
UPC_XA_DBG_UART_TX
UPC_XA_DBG_UART_RX
R3088 OMIT
TP_UPC_XB_DBG_UART_TX
TP_UPC_XB_DBG_UART_RX
ACE Debug Support
Ridge PDs
DP_X_SNK0_DDC_CLK
DP_X_SNK0_DDC_DATA
DP_X_SNK1_DDC_CLK
DP_X_SNK1_DDC_DATA
R3067 100K
R3068 100K
R3069 100K
R3070 100K
NC ALIASES / NO TEST
NC_UPC_XB_I2C_ADDR
GND ALIASES
GND
RIDGE DEBUG CONN
Place on bottom
J3001
505070-1220
USBC_DBG
TBT_X_CIO_PLUG_EVENT_L
DP_X_SNK0_HPD
DP_X_SNK1_HPD
DP_XA_HPD
TBT_POC_RESET
PP3V3_TBT_X_LC
TBT_X_PCI_RESET_L
USBC_X_RESET_L
PP3V3_S5_TBT_X_SW
PP0V9_TBT_X_PCIE
PP0V9_TBT_X_USB
PP0V9_TBT_X_CIO
ACE DEBUG CONN
Place on bottom
J3000
505070-1220
I2C_TBT_XB_INT_L
I2C_UPC_X_SCL2
I2C_UPC_X_SDA2
SMC_USBC_INT_L
TBT_X_SPI_CLK_DBG
UPC_XA_UART_TX
I2C_TBT_XA_INT_L
I2C_TBT_X_SDA
I2C_TBT_X_SCL
I2C_UPC_XA_DBG_CTL_SDA
I2C_UPC_XA_DBG_CTL_SCL
UPC_XA_UART_RX
RIDGE JTAG ISOLATION
JTAG_TBT_TCK
JTAG_TBT_TDI
R3043 0
R3044 0
JTAG_ISP_TCK
JTAG_ISP_TDI
TP_UPC_XA_SWD_DATA
TP_UPC_XA_SWD_CLK
TP_UPC_XB_SWD_DATA
TP_UPC_XB_SWD_CLK
TP3001
TP3002
TP3003
TP3004
POWER ALIASES
PP3V3_UPC_XB_LDO
PP3V3_UPC_XA_LDO
PP20V_USBC_XA_VBUS
PP20V_USBC_XB_VBUS
PPDCIN_G3H
PP5V_S4_X_USBC
PP3V3_TBT_X_S0
ACE A RPD STRAPPING
USBC_XA_CC1
USBC_XA_CC2
ACE B RPD STRAPPING
USBC_XB_CC1
USBC_XB_CC2
ACE PDs
UPC_XA_HPD_RX
UPC_XB_HPD_RX
R3033 100K
R3034 100K
R3035 0
R3036 0
SMC_RESET_L
USB_UPC_XA_P
USB_UPC_XA_N
R3081 0
R3082 0
R3084 0
R3085 0
USB_UPC_XB_P
USB_UPC_XB_N
SIGNAL ALIASES
UPC_X_5V_EN
USB2_UPC_XB_P
USB2_UPC_XB_N
R3086 0
R3087 0
USB_UPC_PCH_XB_P
USB_UPC_PCH_XB_N
TBT_X_CIO_PWR_EN
TBT_X_USB_PWR_EN
PM_BATLOW_L
SMC_PME_S4_DARK_L
UPC_X_SPI_CLK
UPC_X_SPI_CS_L
UPC_X_SPI_MOSI
UPC_X_SPI_MISO
UPC_T_SPI_CLK
UPC_T_SPI_CS_L
UPC_T_SPI_MOSI
UPC_T_SPI_MISO
JTAG_ISP_TDO
SMC_USBC_INT_L
TBT_POC_RESET
TBT_X_CIO_PLUG_EVENT_L
UPC_XA_FAULT_L
UPC_XB_FAULT_L
R3078 0
R3079 0
XDP_PCH_OBSDATA_C0
XDP_PCH_OBSDATA_C1
JTAG_TBT_X_TMS
JTAG_TBT_T_TMS
PP3V3_S4
SMC MOJO
SMC_DEBUGPRT_TX_L
SMC_DEBUGPRT_RX_L
TP_USBC_XA_RESET_L
DCI
PCH USB3
USB3_EXTA_D2R_P
USB3_EXTA_D2R_N
USB3_EXTA_R2D_P
USB3_EXTA_R2D_N
C3020 0.1UF
C3021 0.1UF
USB2_UPC_XA_P
USB2_UPC_XA_N
R3076 0
R3077 0
USB_UPC_PCH_XA_P
USB_UPC_PCH_XA_N
I2C SERIES R'S
I2C_UPC_X_SDA2
I2C_UPC_X_SCL2
R3041 33
R3042 33
SMBUS_SMC_4_G3H_SDA
SMBUS_SMC_4_G3H_SCL
RIDGE 0.9V SVR XW
XW3000
P0V9_TBT_X_SVR_AGND
NO_XNET_CONNECTION=1
TBT to ACE
TBT
Alpine Ridge U2800
(MASTER)
I2C_TBT_X_SCL
I2C_TBT_X_SDA
I2C_TBT_XA_INT_L
I2C_TBT_XB_INT_L
Pri ACE
U3100
(Write: 0x70 Read: 0x71)
Sec ACE
U3200
(Write: 0x7E Read: 0x7F)
Ridge PCIE Caps
PCIE_TBT_X_R2D_C_P<0>
PCIE_TBT_X_R2D_C_N<0>
PCIE_TBT_X_R2D_C_P<1>
PCIE_TBT_X_R2D_C_N<1>
PCIE_TBT_X_R2D_C_P<2>
PCIE_TBT_X_R2D_C_N<2>
PCIE_TBT_X_R2D_C_P<3>
PCIE_TBT_X_R2D_C_N<3>
PCIE_TBT_X_D2R_C_P<0>
PCIE_TBT_X_D2R_C_N<0>
PCIE_TBT_X_D2R_C_P<1>
PCIE_TBT_X_D2R_C_N<1>
PCIE_TBT_X_D2R_C_P<2>
PCIE_TBT_X_D2R_C_N<2>
PCIE_TBT_X_D2R_C_P<3>
PCIE_TBT_X_D2R_C_N<3>
C3040
C3041
C3042
C3043
C3044
C3045
C3046
C3047
C3050
C3051
C3052
C3053
C3054
C3055
C3056
C3057
0.22UF
BOM_COST_GROUP=TBT
PAGE TITLE
USB-C Support
Apple Inc.
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 30 OF 145
SHEET 29 OF 121
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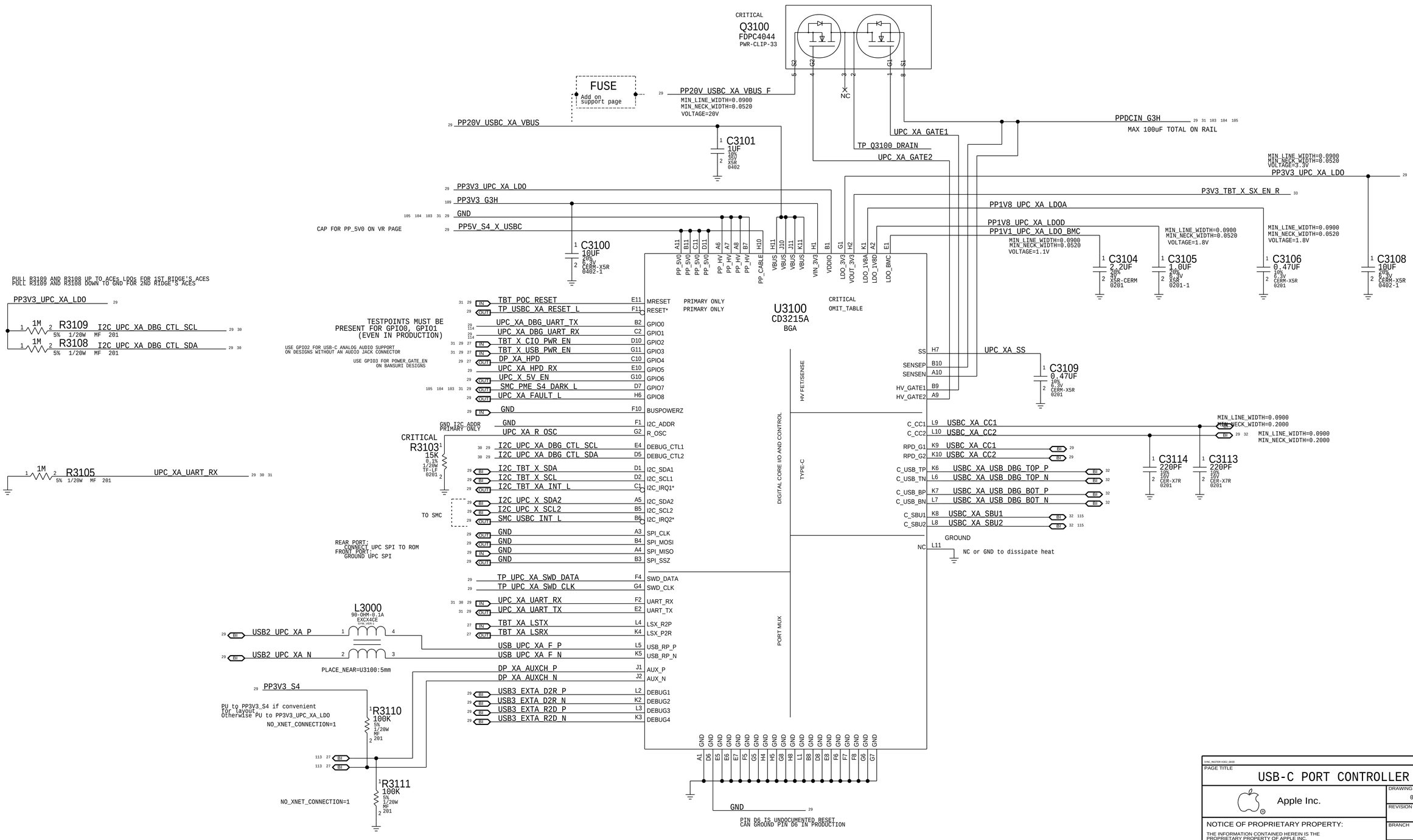
PRIMARY ACE USB-C PORT CONTROLLER (UPC)



BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C PORT CONTROLLER A

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
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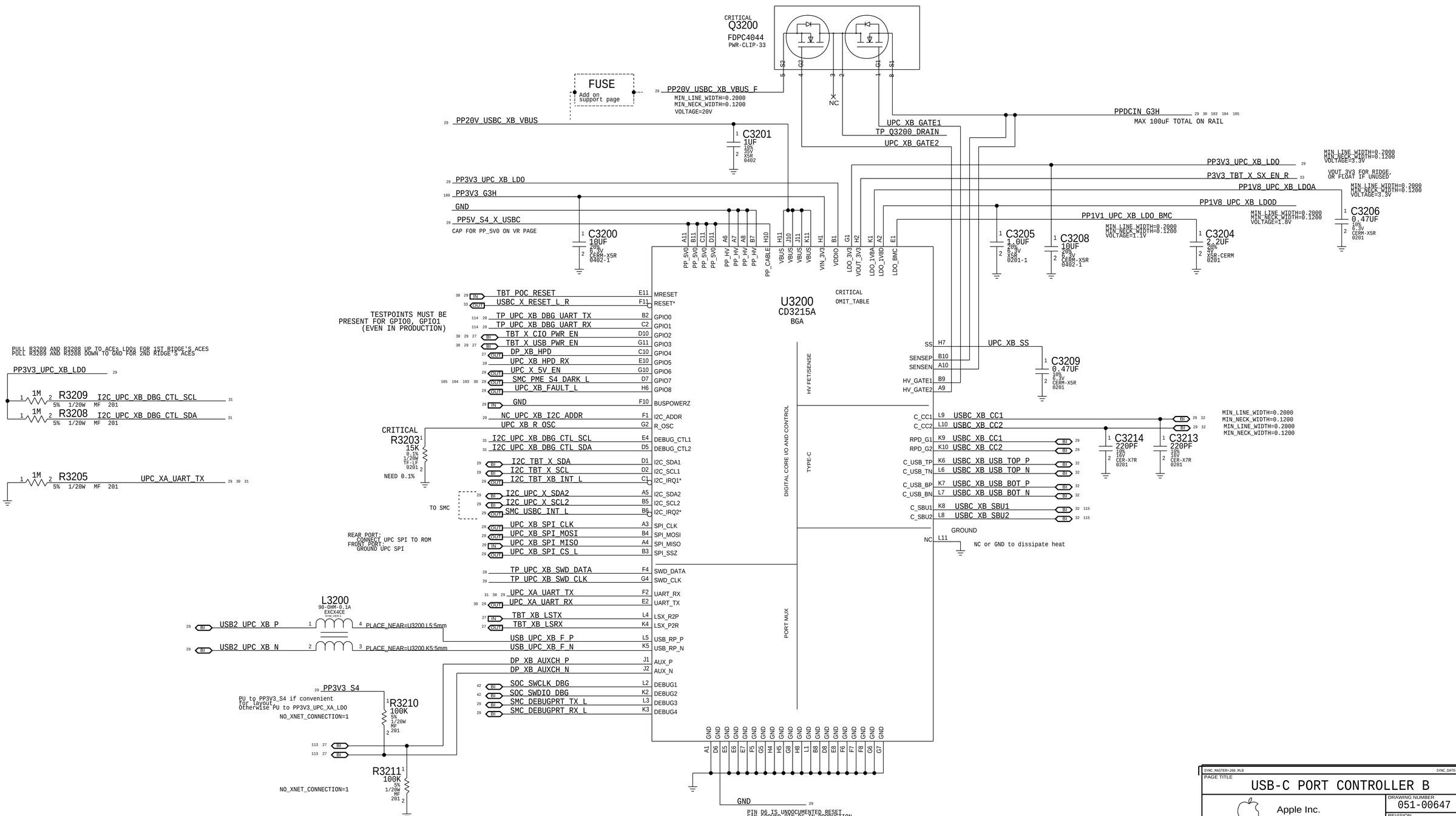
SECONDARY ACE USB-C PORT CONTROLLER (UPC)



BOM_COST_GROUP=USB-C

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE
USB-C PORT CONTROLLER B

Apple Inc.

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SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
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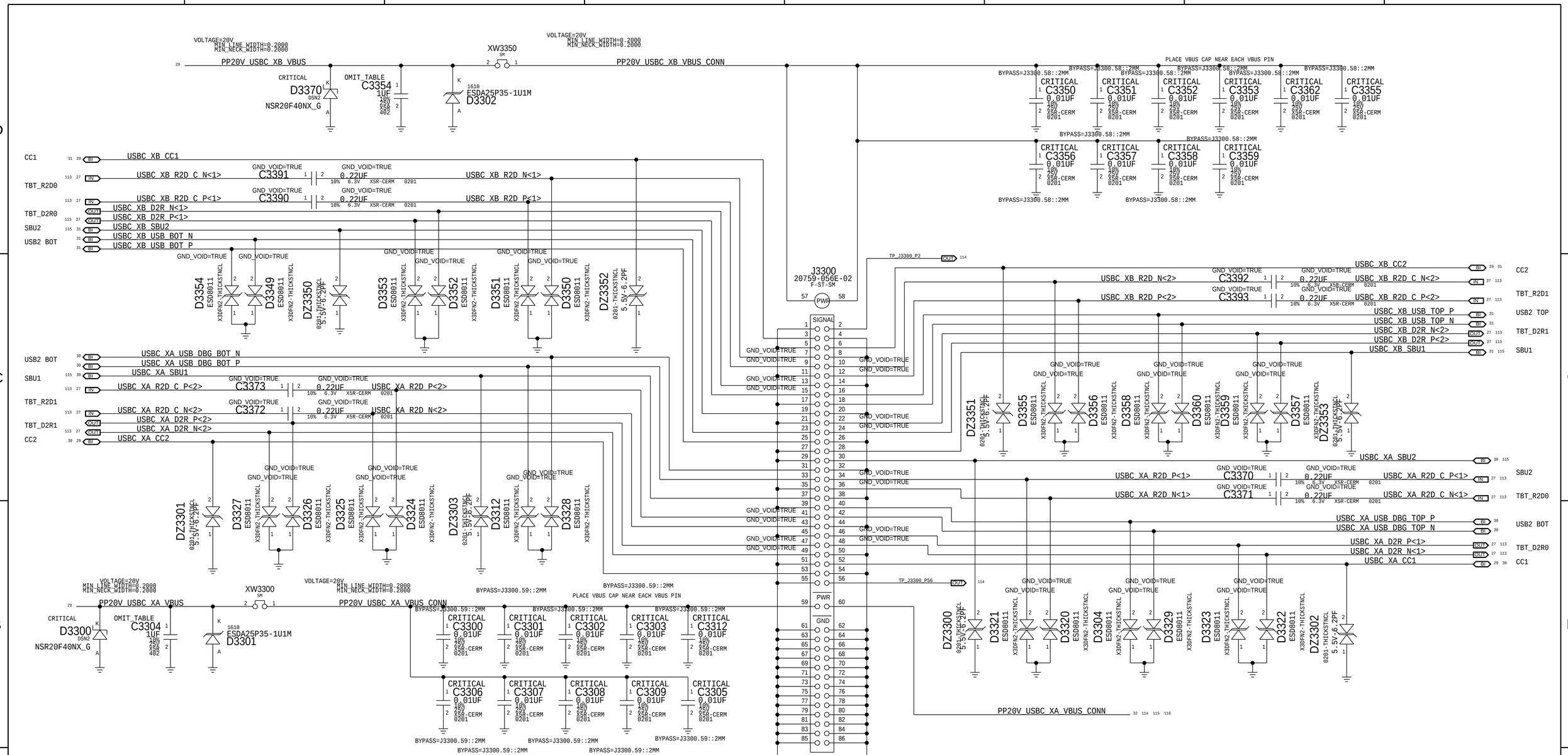

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0683	2	CAP,CER,X5R,1UF,10%,25V,0402	C3304, C3354	CRITICAL	NOSTUFF

BOM_COST_GROUP=USB-C

LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE
USB-C CONNECTOR A

Apple Inc.

DRAWING NUMBER 051-00647
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BRANCH dvt-fab10
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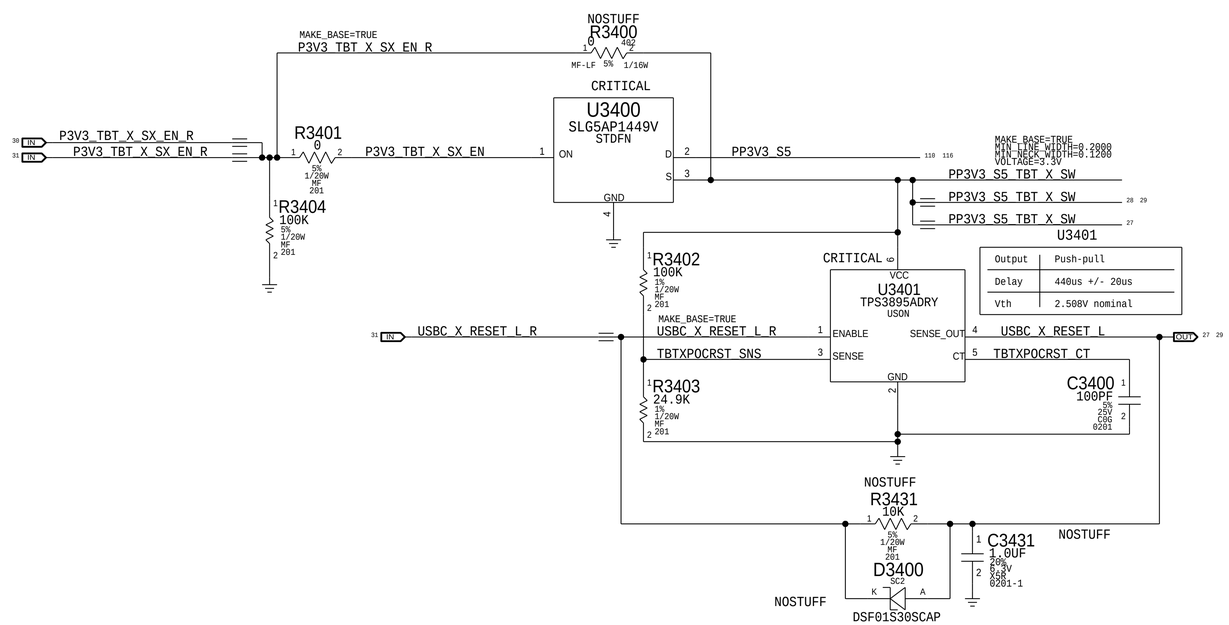
TBT X "POC" Power-up Reset



BOM_COST_GROUP=USB-C

DESIGN: X502/DEV_MLB_U
LAST CHANGE: Wed Feb 18 17:12:24 2015

SYNC_MASTER=X502_MLB SYNC_DATE=03/29/2016

PAGE TITLE
USB-C CONNECTOR B

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DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
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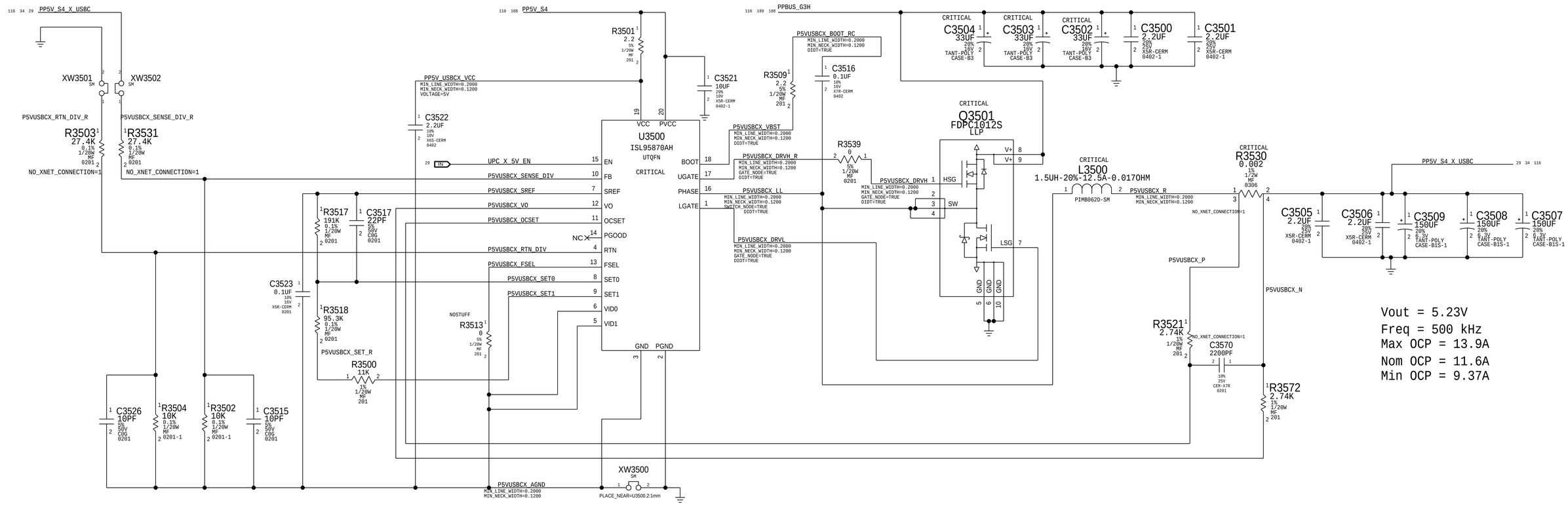

BOM_COST_GROUP=USB-C

SYNC_MASTER=J80_ZIFENGSHEN_MLB_BAFFIN SYNC_DATE=12/04/2015

PAGE TITLE

TBT 5V REGULATOR

Apple Inc.

DRAWING NUMBER	051-00647
SIZE	D
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BRANCH	dvt-fab10
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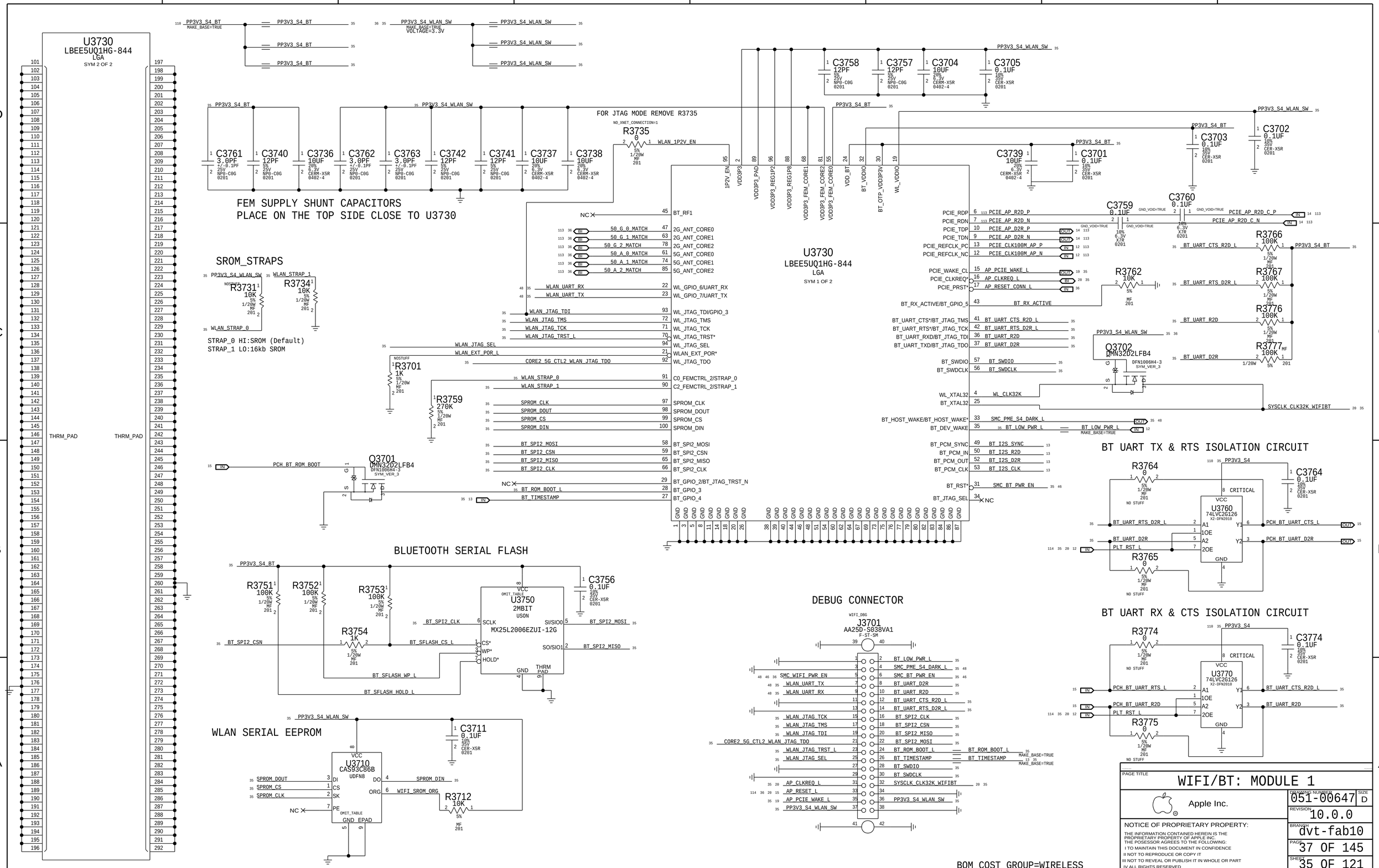
U3730
LBEE5UQ1HG-844
LGA
SYM 2 OF 2
THRM_PAD
FEM SUPPLY SHUNT CAPACITORS
PLACE ON THE TOP SIDE CLOSE TO U3730
FOR JTAG MODE REMOVE R3735
SROM_STRAPS
STRAP_0 HI:SROM (Default)
STRAP_1 LO:16kb SROM
U3730
LBEE5UQ1HG-844
LGA
SYM 1 OF 2
BT UART TX & RTS ISOLATION CIRCUIT
BLUETOOTH SERIAL FLASH
MX25L2006EZUI-12G
DEBUG CONNECTOR
J3701
AA25D-S038VA1
WLAN SERIAL EEPROM
BOM_COST_GROUP=WIRELESS
BT UART RX & CTS ISOLATION CIRCUIT
PAGE TITLE
WIFI/BT: MODULE 1
Apple Inc.
DRAWING NUMBER
051-00647
SIZE
D
REVISION
10.0.0
BRANCH
dvt-fab10
PAGE
37 OF 145
SHEET
35 OF 121
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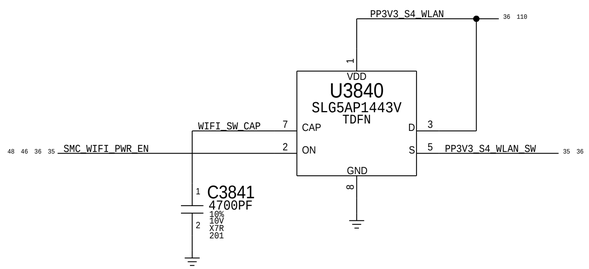
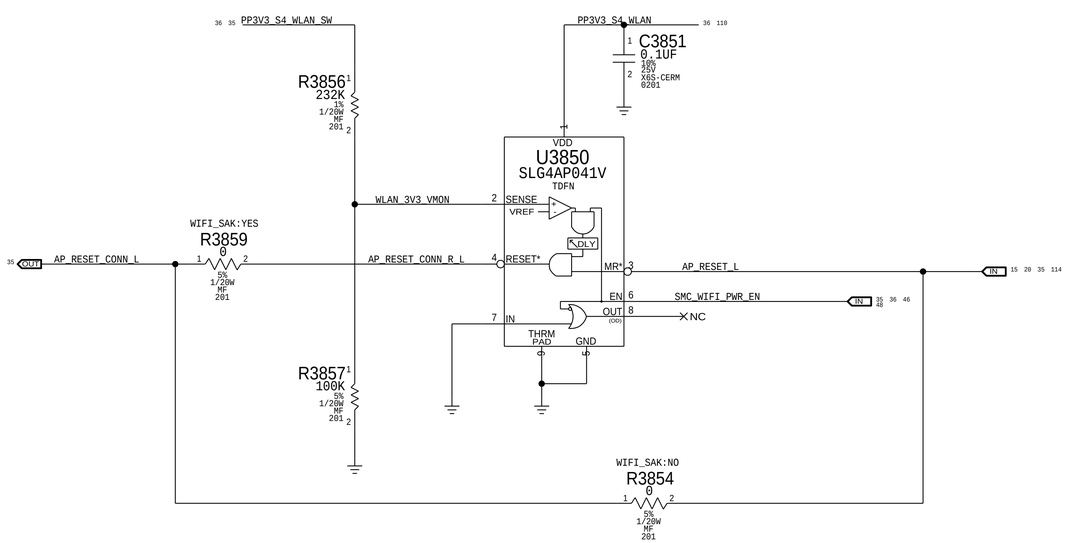
WLAN Power Switch

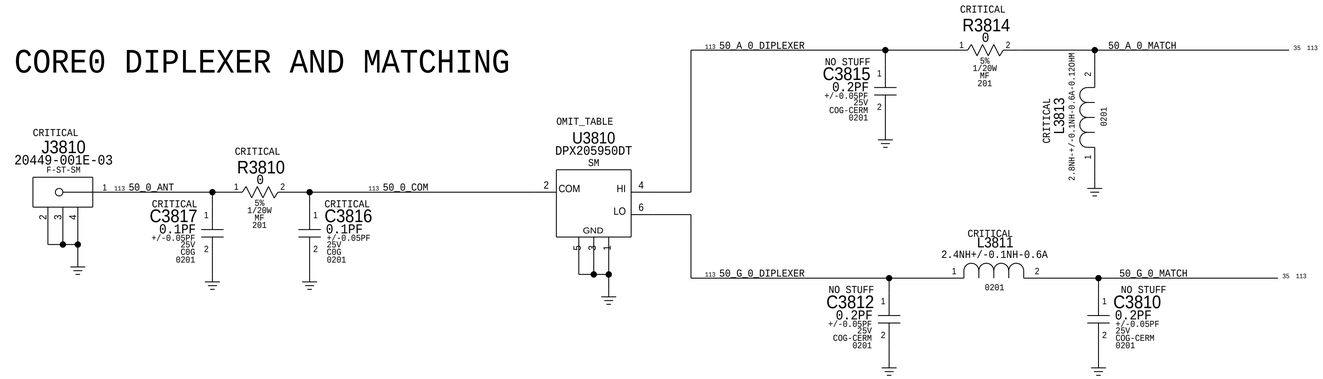


Supervisor & CLKREQ# Isolation

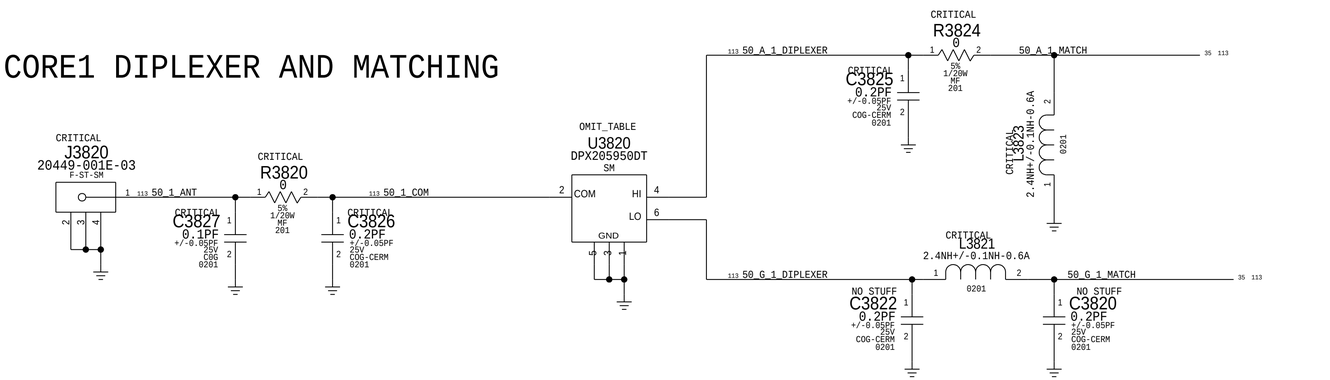
Delay = 130ms +/- 20%



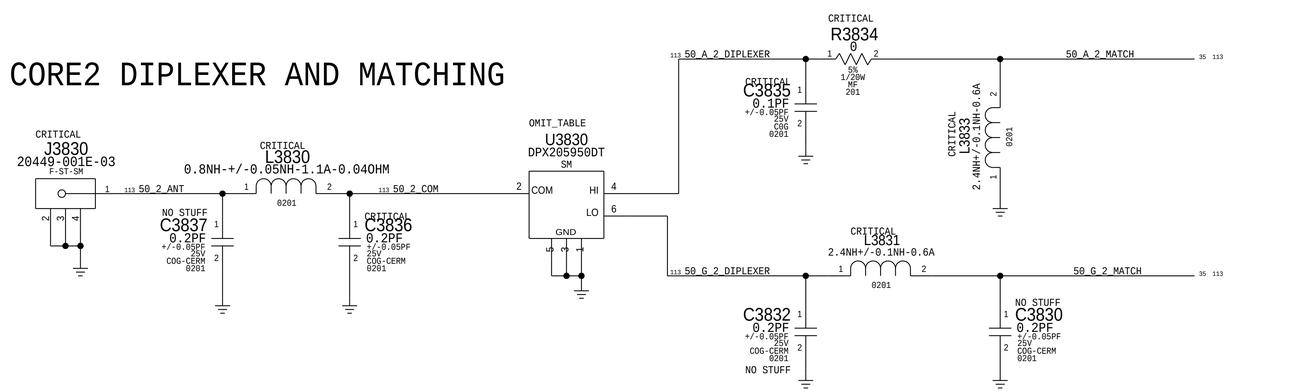
CORE0 DIPLEXER AND MATCHING



CORE1 DIPLEXER AND MATCHING



CORE2 DIPLEXER AND MATCHING



BOM_COST_GROUP=WIRELESS

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE
WIFI/BT: MODULE 2

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

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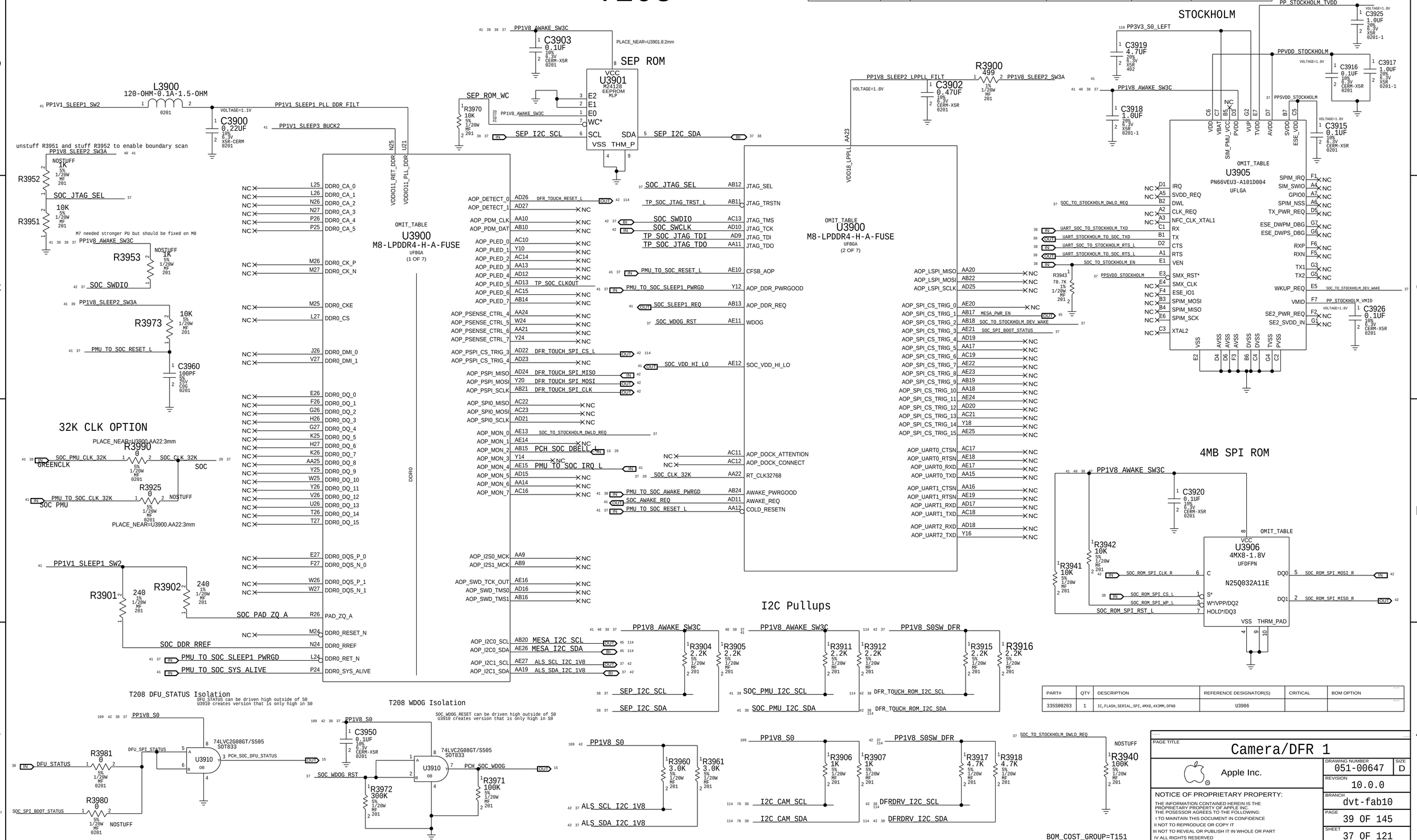
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S00136	1	IC,M8+512MB 20NM DDR,A12,S,SCK,BGA700	U3900	CRITICAL	SOC:HYNIX

T208

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00147	1	IC,RTM2,DEV,PN549A1,P61D0	U3905	CRITICAL	SE:DEV
338S00097	1	IC,RTM2,MP,PN549A1,P61D0	U3905	CRITICAL	SE:PROD



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00203	1	IC,FLASH,SERIAL,SPI,4MX8,4X3MM,DFN8	U3906		

PAGE TITLE

Camera/DFR 1

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

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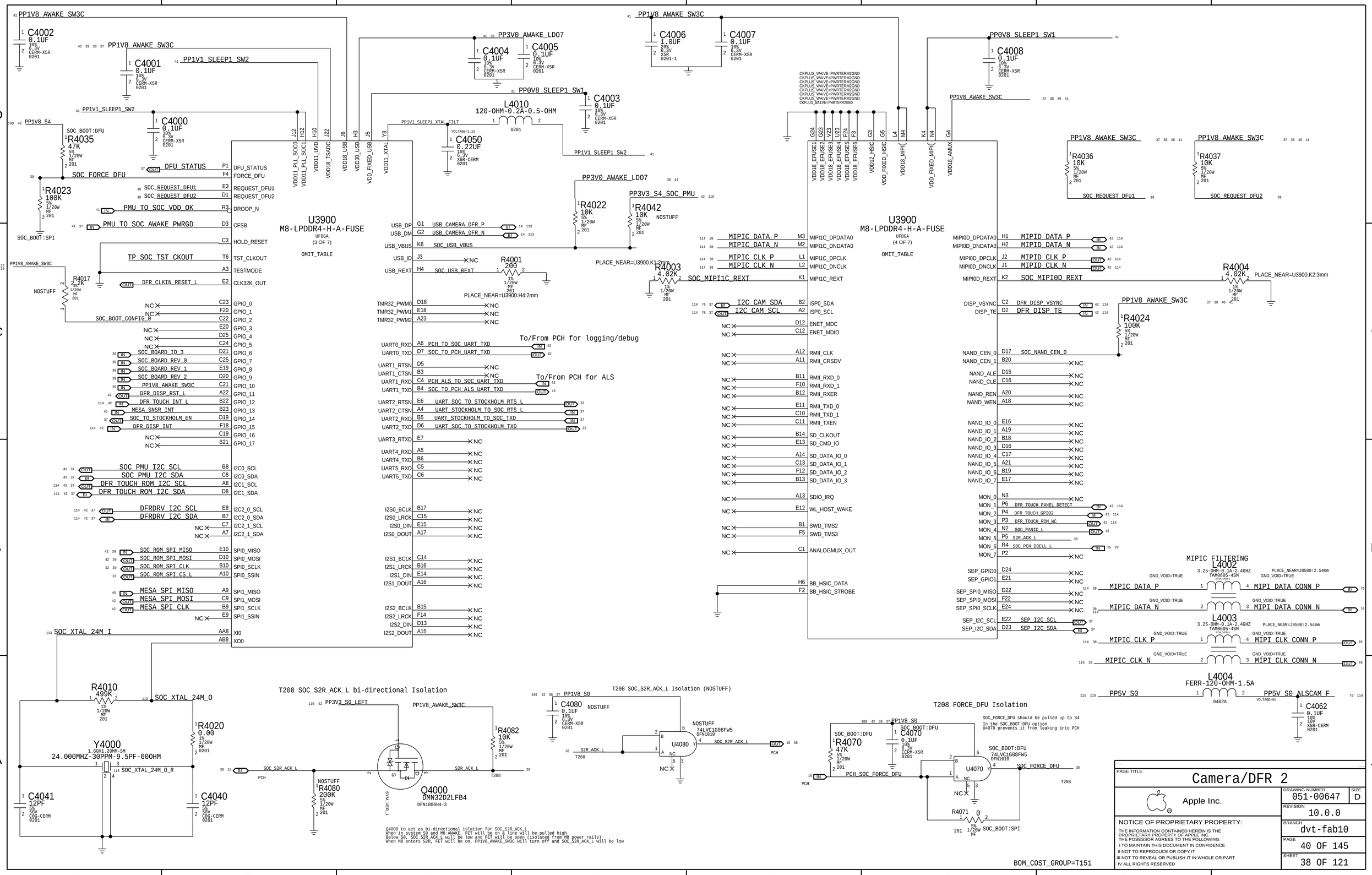
U3900
M8-LPDDR4-H-A-FUSE
UFBGA
(3 OF 7)
OMIT_TABLE
U3900
M8-LPDDR4-H-A-FUSE
UFBGA
(4 OF 7)
OMIT_TABLE
PP1V8_AWAKE_SW3C
PP1V1_SLEEP1_SW2
PP3V0_AWAKE_LDO7
PP0V8_SLEEP1_SW1
PP1V1_SLEEP1_XTAL_FILT
PP3V3_S4_SOC_PMU
L4010
120-OHM-0.2A-0.5-OHM
C4050
0.22UF
R4035
47K
R4023
100K
R4017
2.2K
NOSTUFF
R4022
10K
R4042
10K
NOSTUFF
R4001
200
R4003
4.02K
R4004
4.02K
R4036
10K
R4037
10K
R4024
100K
DFU_STATUS
SOC_FORCE_DFU
SOC_REQUEST_DFU1
SOC_REQUEST_DFU2
PMU_TO_SOC_VDD_OK
PMU_TO_SOC_AWAKE_PWRGD
TP_SOC_TST_CKOUT
DFR_CLKIN_RESET_L
SOC_BOOT_CONFIG_0
SOC_BOARD_ID_3
SOC_BOARD_REV_0
SOC_BOARD_REV_1
SOC_BOARD_REV_2
DFR_DISP_RST_L
DFR_TOUCH_INT_L
MESA_SNSR_INT
SOC_TO_STOCKHOLM_EN
DFR_DISP_INT
SOC_PMU_I2C_SCL
SOC_PMU_I2C_SDA
DFR_TOUCH_ROM_I2C_SCL
DFR_TOUCH_ROM_I2C_SDA
DFRDRV_I2C_SCL
DFRDRV_I2C_SDA
SOC_ROM_SPI_MISO
SOC_ROM_SPI_MOSI
SOC_ROM_SPI_CLK
SOC_ROM_SPI_CS_L
MESA_SPI_MISO
MESA_SPI_MOSI
MESA_SPI_CLK
SOC_XTAL_24M_I
USB_CAMERA_DFR_P
USB_CAMERA_DFR_N
SOC_USB_VBUS
SOC_USB_REXT
PLACE_NEAR=U3900.H4:2mm
To/From PCH for logging/debug
PCH_TO_SOC_UART_TXD
SOC_TO_PCH_UART_TXD
To/From PCH for ALS
PCH_ALS_TO_SOC_UART_TXD
SOC_TO_PCH_ALS_UART_TXD
UART_SOC_TO_STOCKHOLM_RTS_L
UART_STOCKHOLM_TO_SOC_RTS_L
UART_STOCKHOLM_TO_SOC_TXD
UART_SOC_TO_STOCKHOLM_TXD
MIPIC_DATA_P
MIPIC_DATA_N
MIPIC_CLK_P
MIPIC_CLK_N
SOC_MIPI1C_REXT
PLACE_NEAR=U3900.K1:2mm
I2C_CAM_SDA
I2C_CAM_SCL
MIPID_DATA_P
MIPID_DATA_N
MIPID_CLK_P
MIPID_CLK_N
SOC_MIPI0D_REXT
PLACE_NEAR=U3900.K2:3mm
DFR_DISP_VSYNC
DFR_DISP_TE
SOC_NAND_CEN_0
DFR_TOUCH_PANEL_DETECT
DFR_TOUCH_GPIO2
DFR_TOUCH_ROM_WC
SOC_PANIC_L
S2R_ACK_L
SOC_PCH_DBELL_L
SEP_I2C_SCL
SEP_I2C_SDA
MIPIC FILTERING
L4002
L4003
3.25-OHM-0.1A-2.4GHZ
TAM0605-4SM
PLACE_NEAR=J8500:2.54mm
MIPIC_DATA_P
MIPIC_DATA_N
MIPIC_CLK_P
MIPIC_CLK_N
MIPI_DATA_CONN_P
MIPI_DATA_CONN_N
MIPI_CLK_CONN_P
MIPI_CLK_CONN_N
L4004
FERR-120-OHM-1.5A
PP5V_S0
PP5V_S0_ALSCAM_F
C4062
0.1UF
R4020
0.00
R4010
499K
Y4000
1.60X1.20MM-SM
24.000MHZ-30PPM-9.5PF-60OHM
C4041
12PF
C4040
12PF
T208 SOC_S2R_ACK_L bi-directional Isolation
PP3V3_S0_LEFT
PP1V8_AWAKE_SW3C
R4082
10K
R4080
200K
Q4000
DMN32D2LFB4
DFN1006H4-3
Q4000 to act as bi-directional islation for SOC_S2R_ACK_L
When in system S0 and M8 AWAKE, FET will be on & line will be pulled high
Below S0, SOC_S2R_ACK_L will be low and FET will be open (isolated from M8 power rails)
When M8 enters S2R, FET will be on, PP1V8_AWAKE_SW3C will turn off and SOC_S2R_ACK_L will be low
T208 SOC_S2R_ACK_L Isolation (NOSTUFF)
C4080
0.1UF
U4080
74LVC1G08FW5
DFN1010
T208 FORCE_DFU Isolation
SOC_FORCE_DFU should be pulled up to S4
In the SOC_BOOT:DFU option
U4070 prevents it from leaking into PCH
R4070
47K
C4070
0.1UF
U4070
74LVC1G08FW5
DFN1010
R4071
0
SOC_BOOT:SPI
BOM_COST_GROUP=T151
PAGE TITLE
Camera/DFR 2
Apple Inc.
DRAWING NUMBER
051-00647
SIZE
D
REVISION
10.0.0
BRANCH
dvt-fab10
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SHEET
38 OF 121
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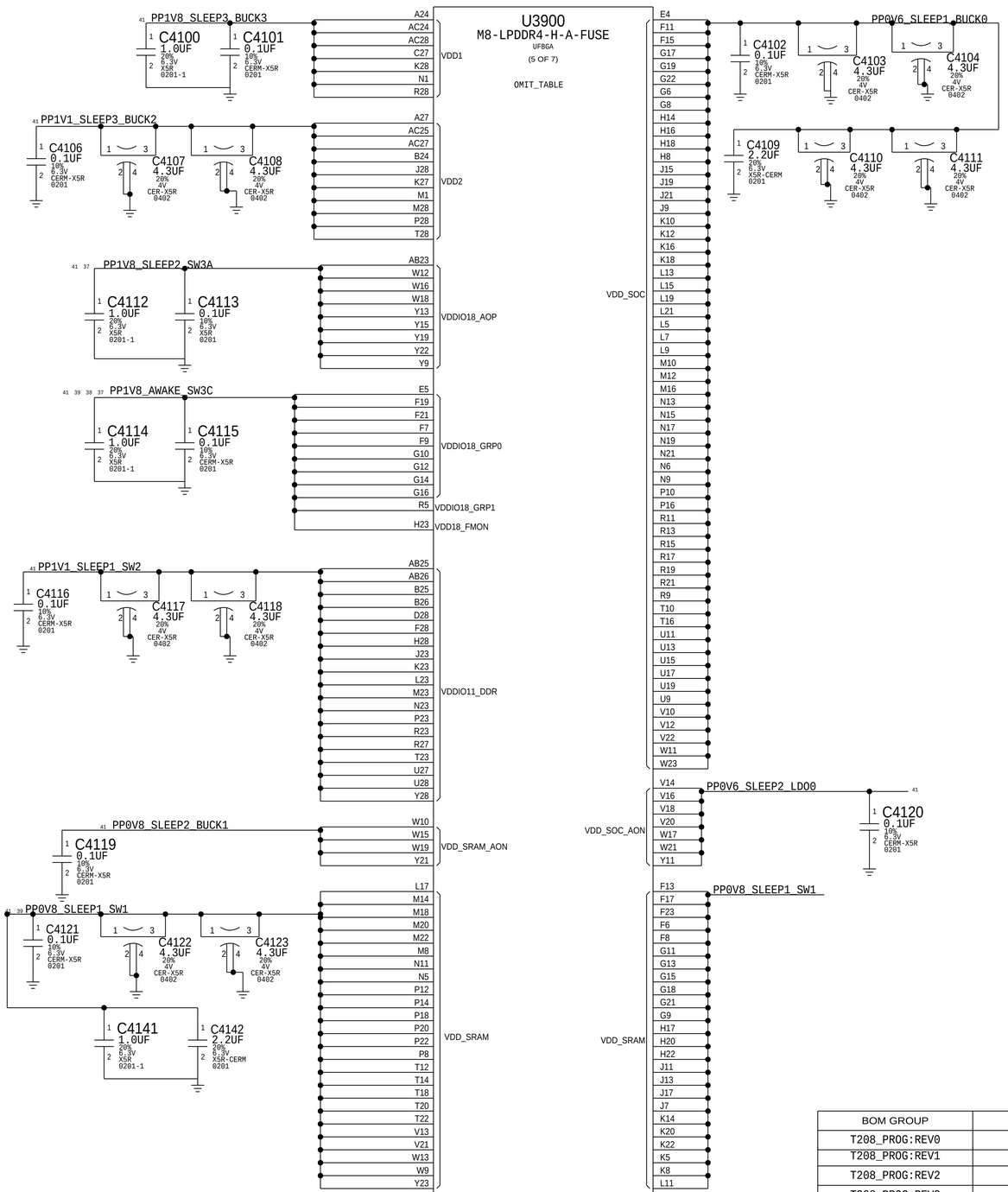
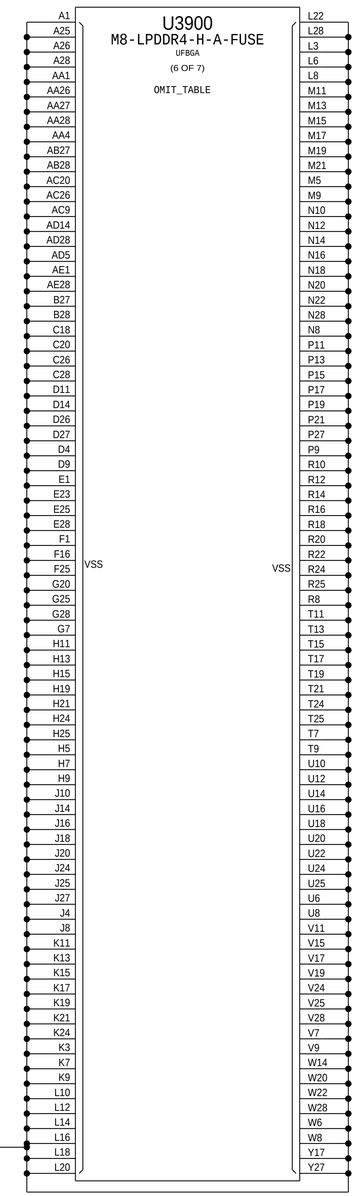
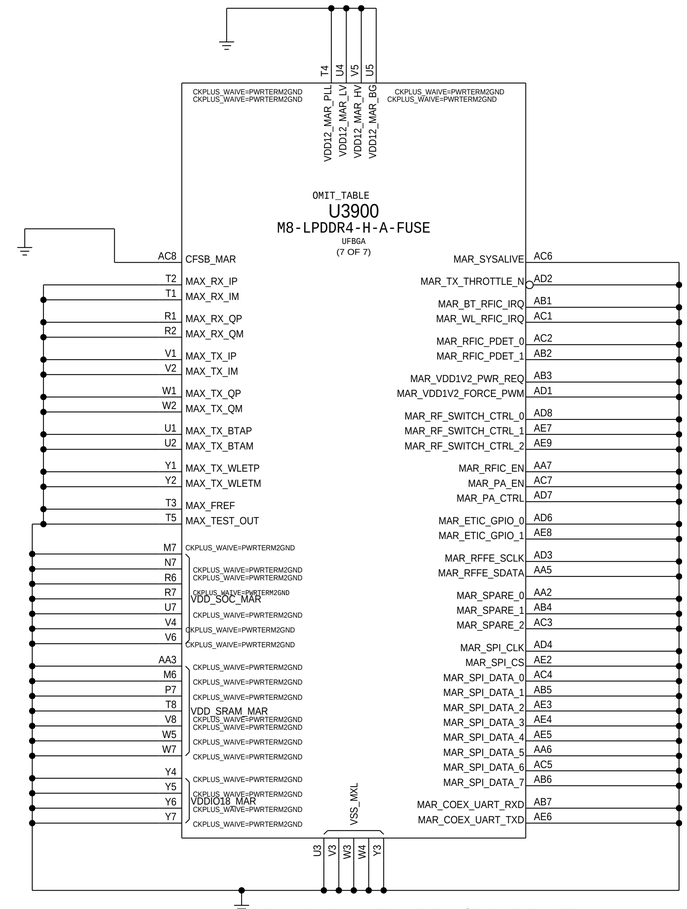


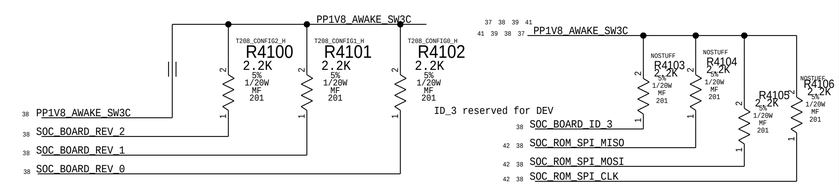




T208 BOARD REV/BOARD ID

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ
4. DISABLE PD AND ENABLE PU



BOARD REV[3:0]	MODE
1111	T208_Rev0 (X362 P0)
1110	T208_Rev1 (X363 P0)
1101	T208_Rev2 (X362 P1)
1100	T208_Rev3 (X362 P2)
1011	T208_Rev4 (X363 P2/X362 localEVT)
1010	T208_Rev5 (X363 EVT/X362 EVT1)

BOARD ID[3:0]	MODE
1XXX	T202 DEV
0010	T208

BOM GROUP	BOM OPTIONS
T208_PROG:REV0	T208_CONFIG2_H,T208_CONFIG1_H,T208_CONFIG0_H
T208_PROG:REV1	T208_CONFIG2_H,T208_CONFIG1_H
T208_PROG:REV2	T208_CONFIG2_H,T208_CONFIG0_H
T208_PROG:REV3	T208_CONFIG2_H
T208_PROG:REV4	T208_CONFIG1_H, T208_CONFIG0_H
T208_PROG:REV5	T208_CONFIG1_H

BOM_COST_GROUP=T151

PAGE TITLE: Camera/DFR 3

Apple Inc.

DRAWING NUMBER: 051-00647 SIZE: D

REVISION: 10.0.0

BRANCH: dvt-fab10

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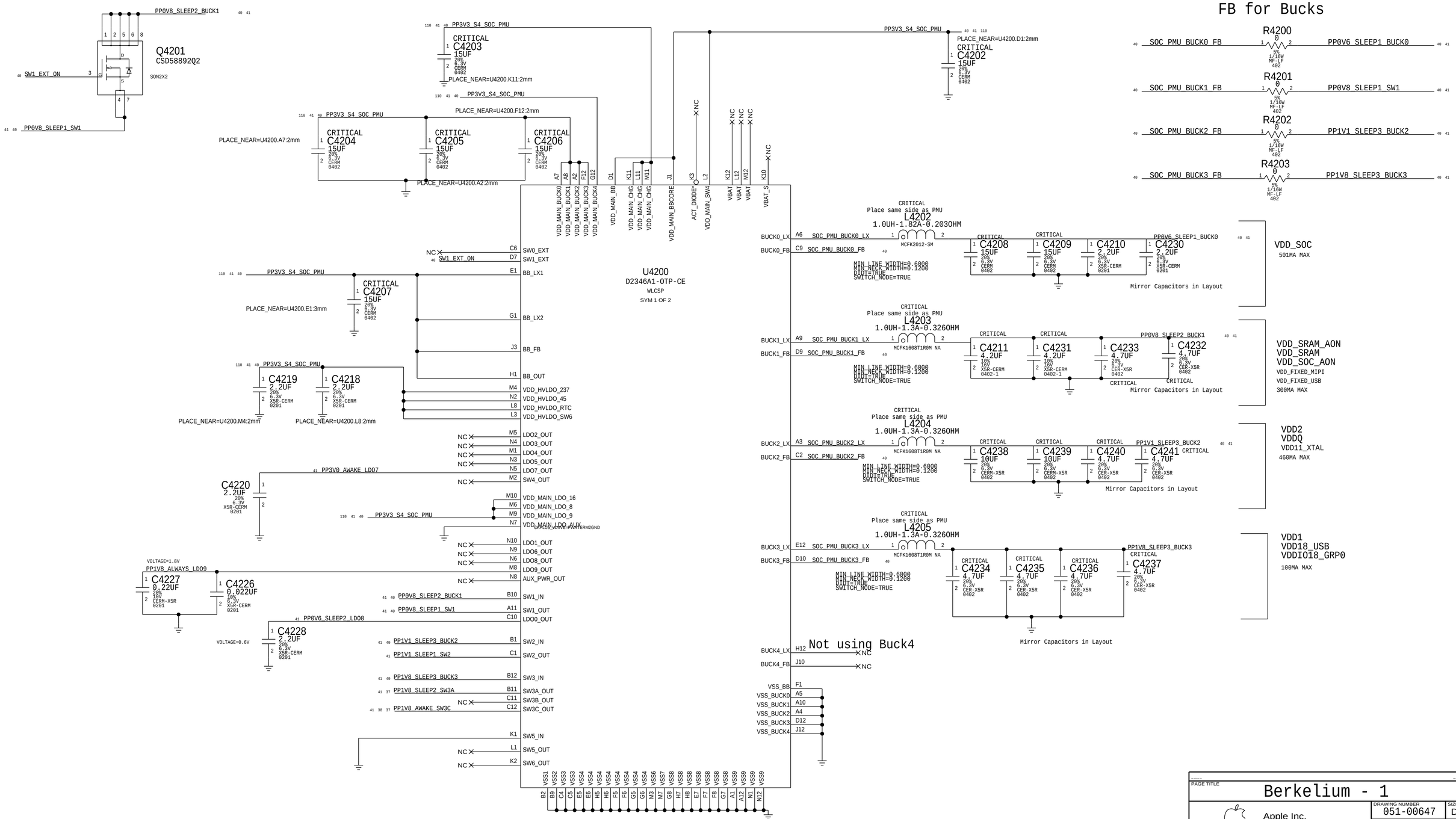
Berkelium



PAGE TITLE	Berkelium - 1
	Apple Inc.
DRAWING NUMBER	051-00647
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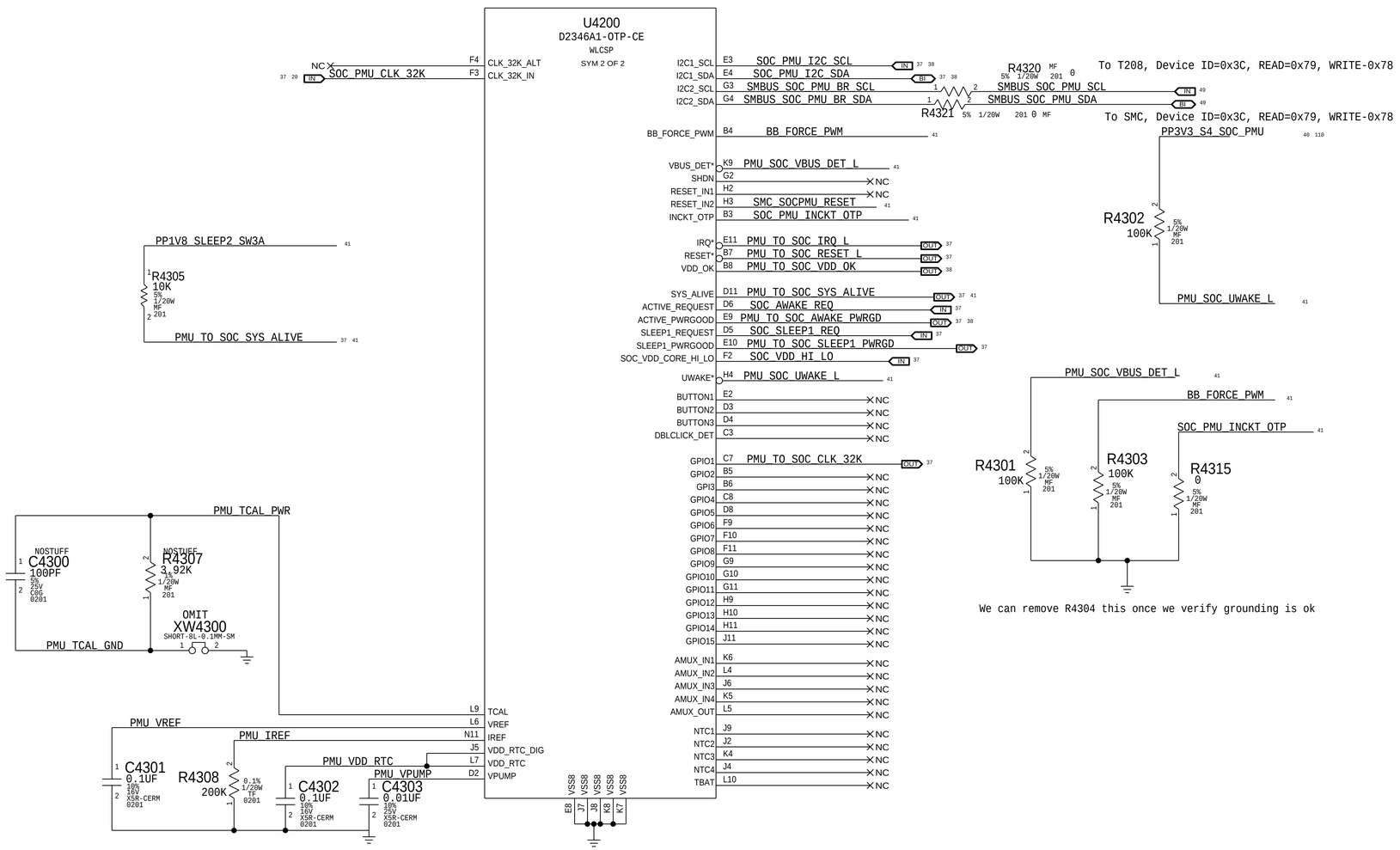
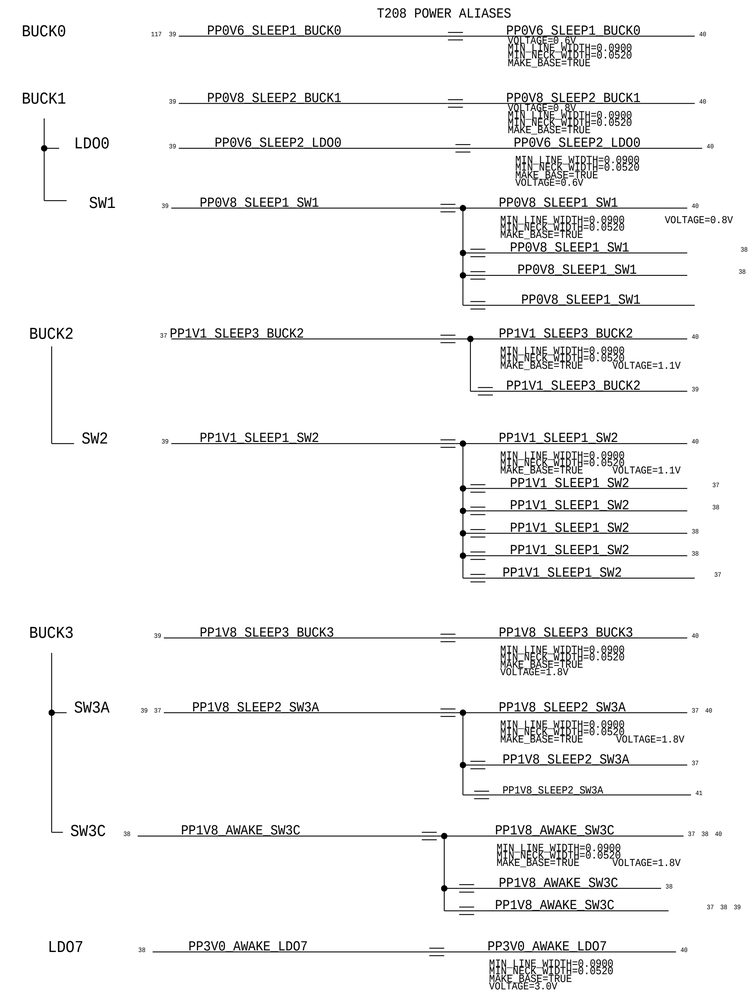
Berkelium - 2





Signal Aliases

SMC_SOCPMU_RESET = SMC_SOCPMU_RESET
MAKE_BASE=TRUE

BOM_COST_GROUP=T151

PAGE TITLE	Berkelium - 2
	Apple Inc.
DRAWING NUMBER	051-00647
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BRANCH	dvt-fab10
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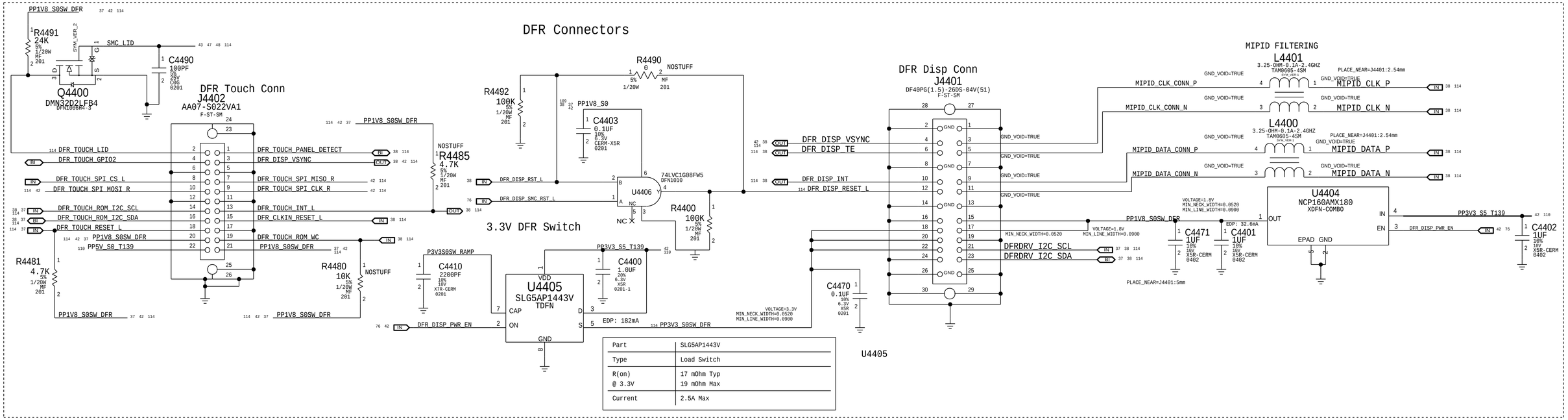
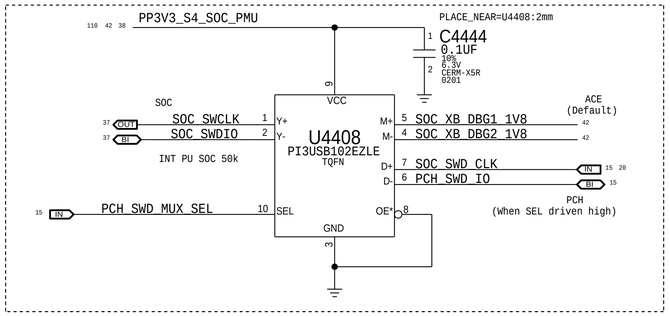
T208 Support



Part	SLG5AP1443V
Type	Load Switch
R(on) @ 3.3V	17 mOhm Typ 19 mOhm Max
Current	2.5A Max

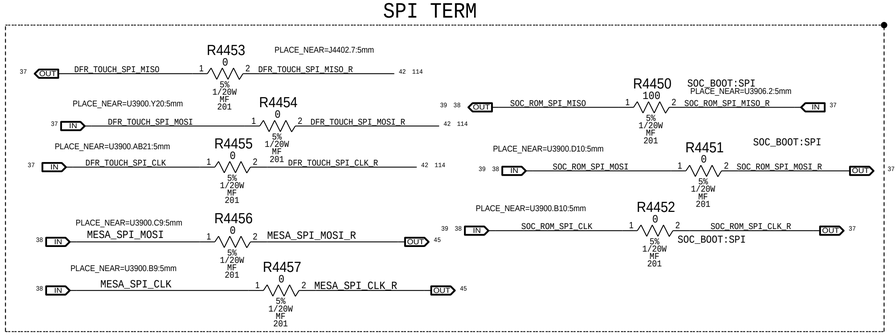
SWD DEBUG MUX



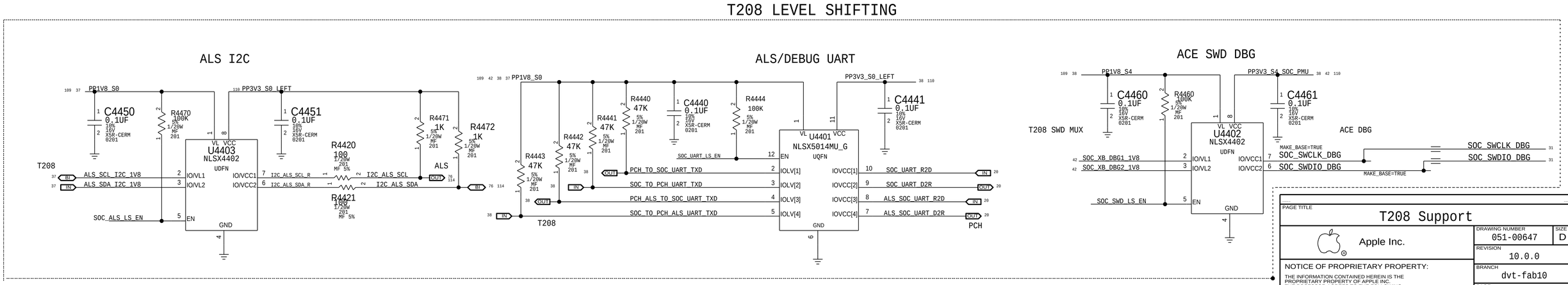
T208 I2C Mapping

Bus	Device	7-bit Address	8-bit Address Read	8-bit Address Write
AP0	PMU	0011110 (0x3C)	0x79	0x78
AP1	Touch EEPROM	1010000 (0x50)	0xA1	0xA0
AP2_0	Tesla	1010100 (0x4C)	0x99	0x98
AOP0	Mesa EEPROM	101000x (0x50/0x51)	0xA1/A3	0xA0/A2
AOP1	ALS	0111001 (0x39)	0x73	0x72
SEP	M34128 EEPROM	1010001 (0x51)	0xA3	0xA2

SPI TERM



T208 LEVEL SHIFTING



PAGE TITLE: T208 Support

Apple Inc.

DRAWING NUMBER: 051-00647 | SIZE: D

REVISION: 10.0.0

BRANCH: dvt-fab10

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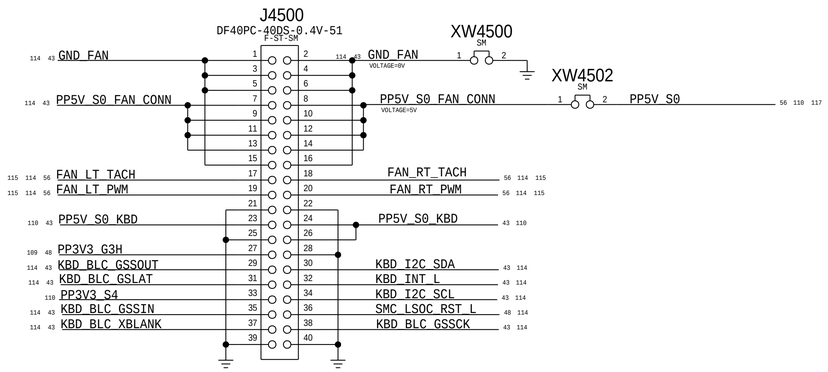
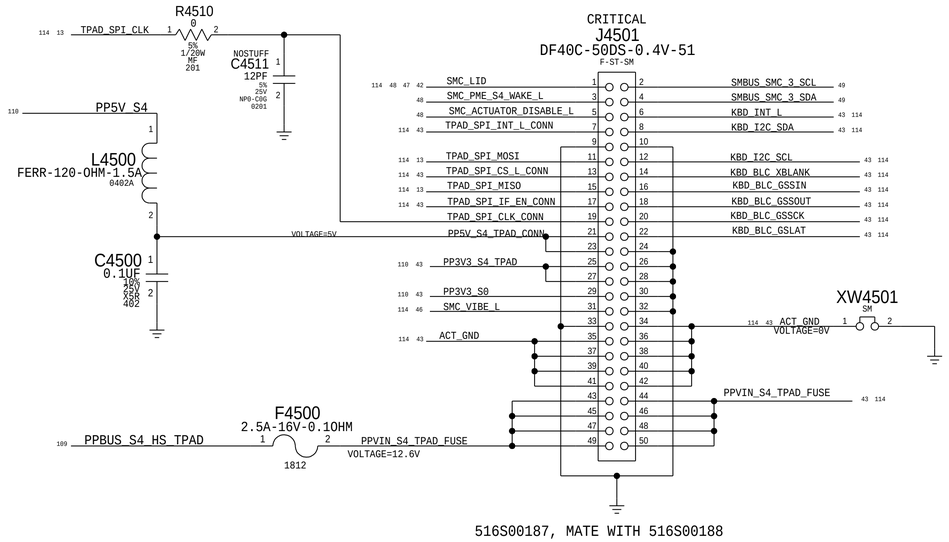
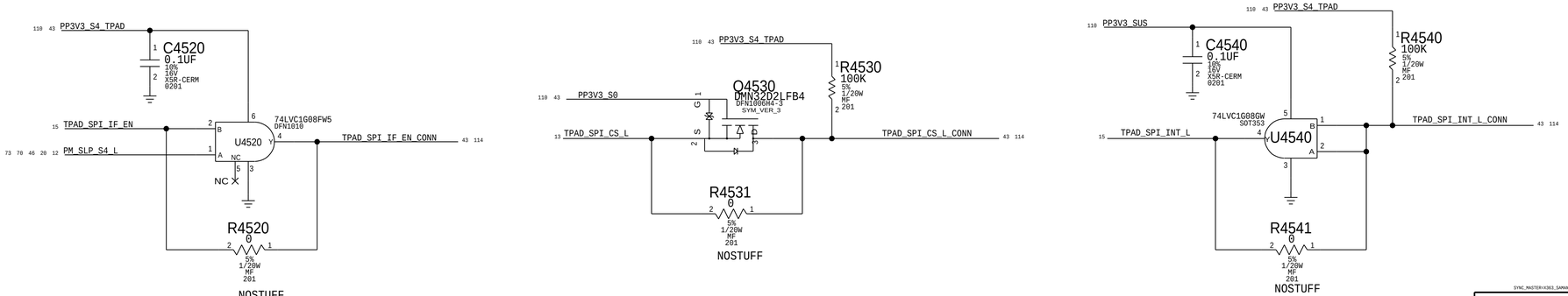
KBD CONNECTOR



TPAD CONNECTOR



TRACKPAD ISOLATION GATES/FET



BOM_COST_GROUP=KEYBOARD

SYNC_MASTER=X363_SAMANTHA SYNC_DATE=01/08/2016

PAGE TITLE
Connectors&ESD

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D
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Debug Stuff Was Here

BOM_COST_GROUP=DEBUG

SYNC_MASTER=J68_MLB SYNC_DATE=08/26/2015

PAGE TITLE

External A USB3 Connector

Apple Inc.

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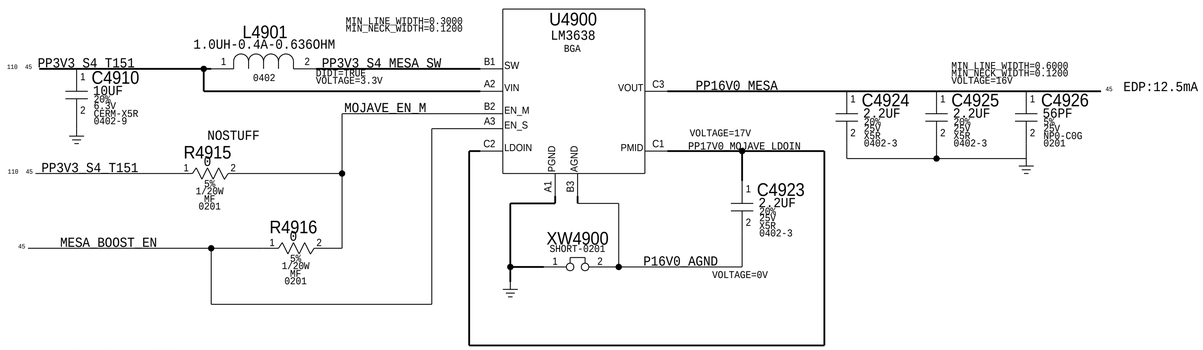
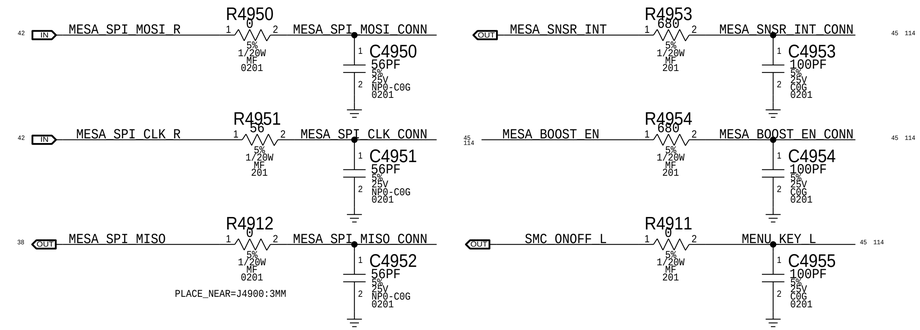
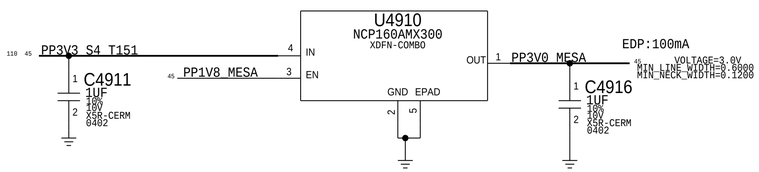
MOJAVE 16V BOOST

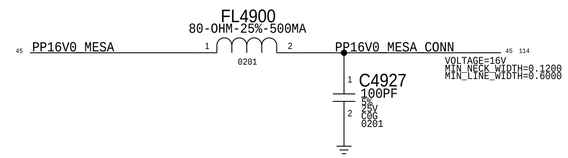




3.0V MESA

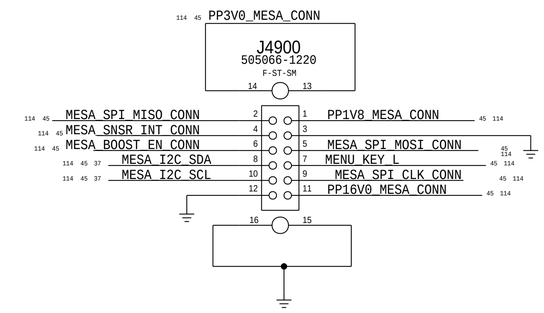
Option to feed LDO from 5V in case of dropout issue





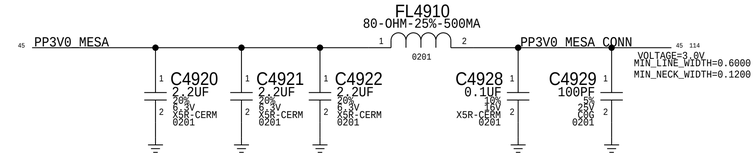
MESA FLEX CONNECTOR

Proto1 Connector for X434/X435 Support
PLUG (516S00115) - X434/ X435 Jumper
Recptacle (516S00203) - X362/X363 MLB

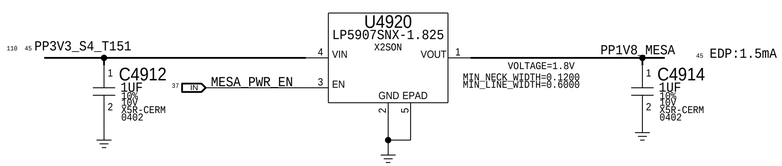


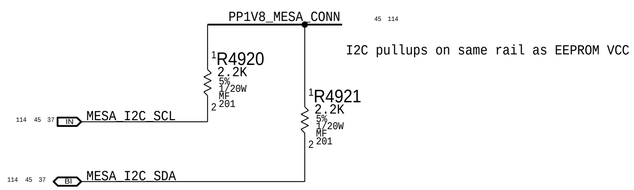
Mesa Power Sequencing Requirements

Power On: 1V8 -> 3V3 -> 16V0

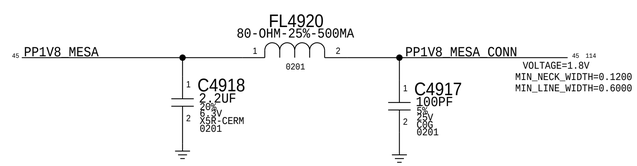


1.8V MESA





I2C pullups on same rail as EEPROM VCC



BOM_COST_GROUP=T151

PAGE TITLE	MESA
Apple Inc.	DRAWING NUMBER 051-00647 SIZE D
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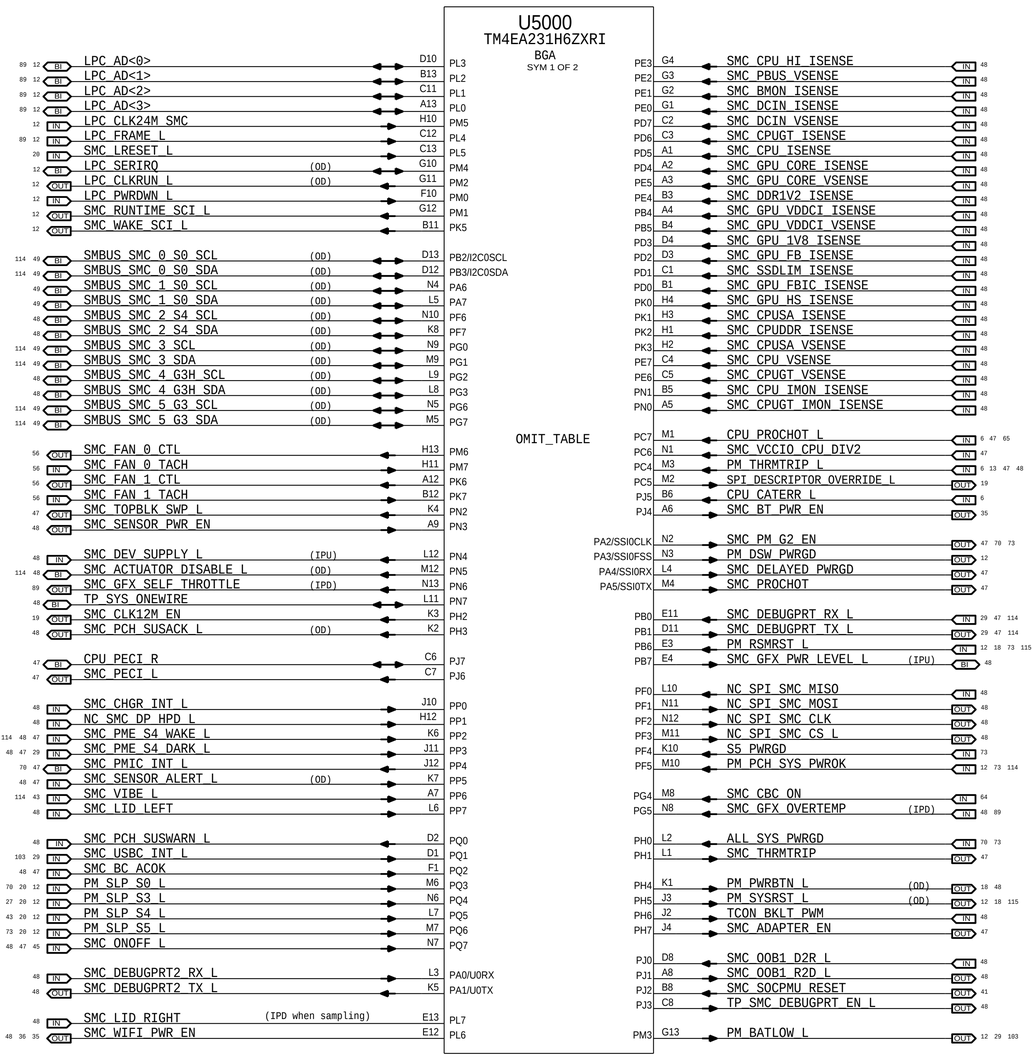

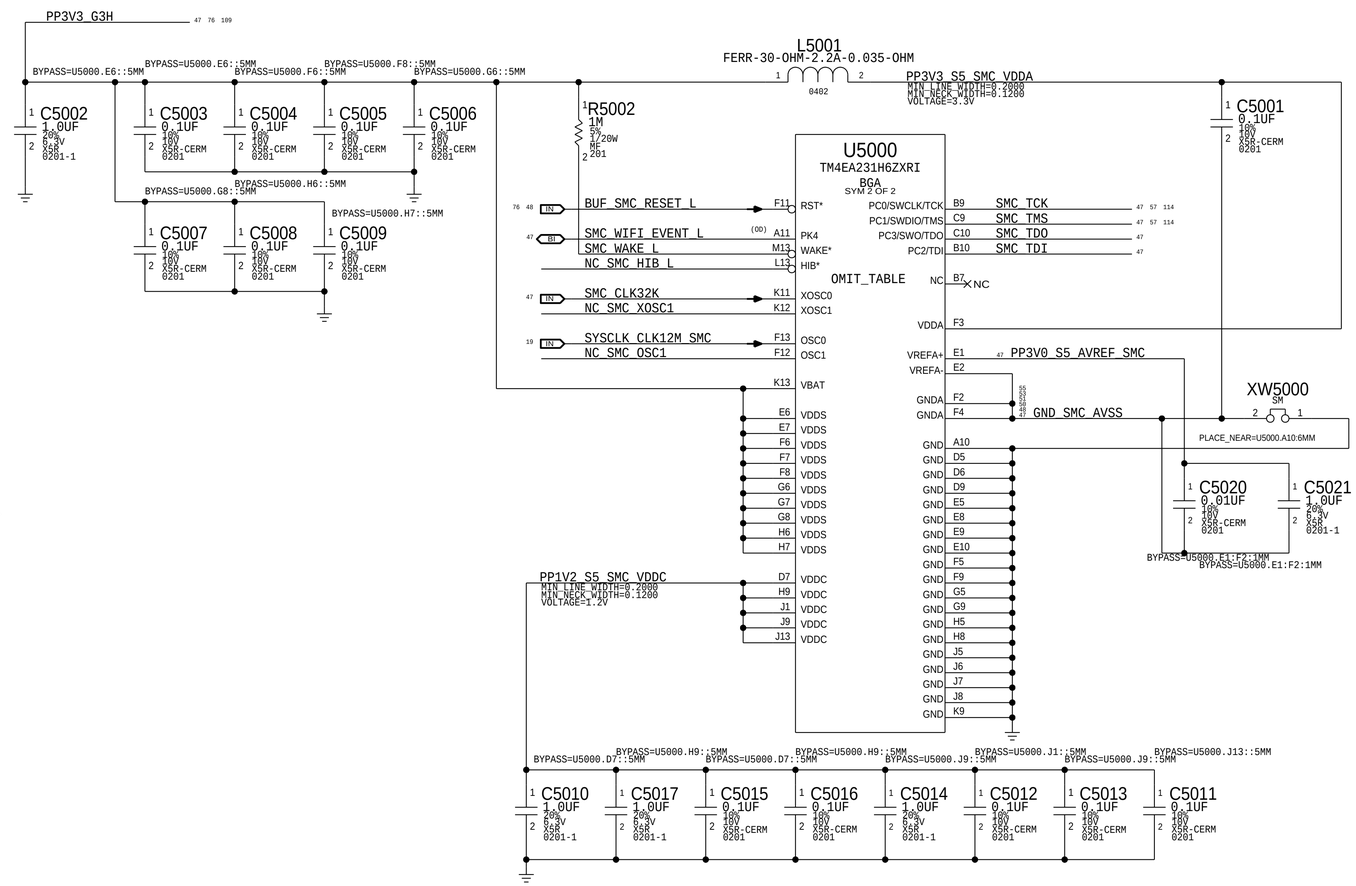

NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

BOM_COST_GROUP=SMC

PAGE TITLE
SMC

Apple Inc.

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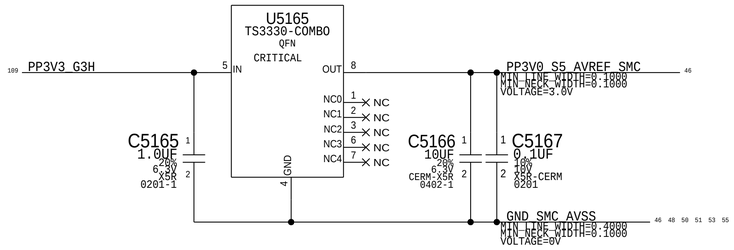
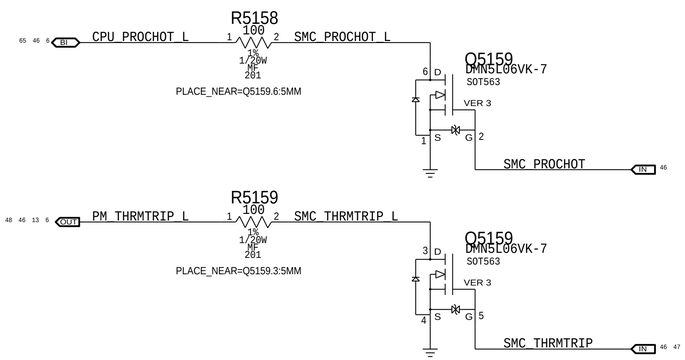
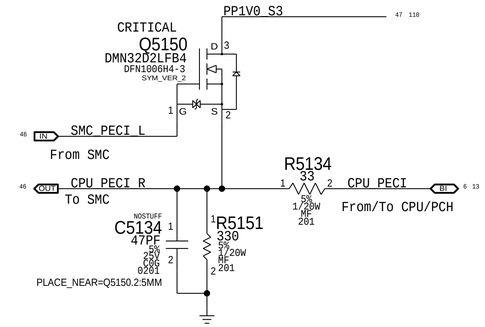
SMC AVREF Supply



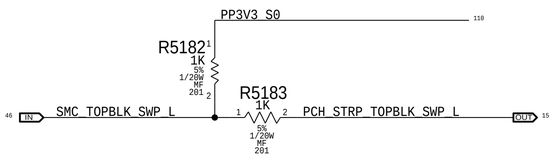
PROCHOT/THRMTRIP Support

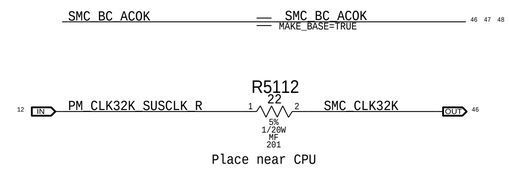


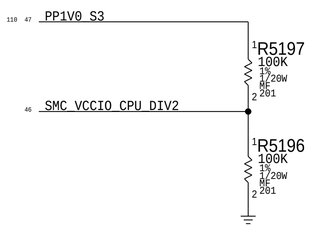
PECI Support

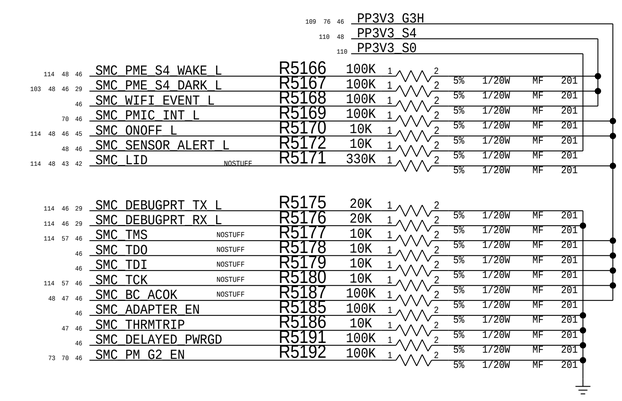


Top-Block Swap









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SYNC_MASTER=J80_ZIFENGSHEN_MLB_BAFFIN SYNC_DATE=11/19/2015

PAGE TITLE

SMC Shared Support

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SMC12 ADC Assignments

SMC_CPU_HI_ISENSE	SMC_CPU_HI_ISENSE	MAKE_BASE=TRUE	
SMC_PBUS_VSENSE	SMC_PBUS_VSENSE	MAKE_BASE=TRUE	
SMC_BMON_ISENSE	SMC_BMON_ISENSE	MAKE_BASE=TRUE	
SMC_DCIN_ISENSE	SMC_DCIN_ISENSE	MAKE_BASE=TRUE	
SMC_DCIN_VSENSE	SMC_DCIN_VSENSE	MAKE_BASE=TRUE	
SMC_CPUGT_ISENSE	SMC_CPUGT_ISENSE	MAKE_BASE=TRUE	
SMC_CPU_ISENSE	SMC_CPU_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_CORE_ISENSE	SMC_GPU_CORE_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_CORE_VSENSE	SMC_GPU_CORE_VSENSE	MAKE_BASE=TRUE	
SMC_DDR1V2_ISENSE	SMC_DDR1V2_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_VDDCI_ISENSE	SMC_GPU_VDDCI_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_VDDCI_VSENSE	SMC_GPU_VDDCI_VSENSE	MAKE_BASE=TRUE	
SMC_GPU_1V8_ISENSE	SMC_GPU_1V8_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_FB_ISENSE	SMC_GPU_FB_ISENSE	MAKE_BASE=TRUE	
SMC_SSDLIM_ISENSE	SMC_SSDLIM_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_FBIC_ISENSE	SMC_GPU_FBIC_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_HS_ISENSE	SMC_GPU_HS_ISENSE	MAKE_BASE=TRUE	
SMC_CPUSA_ISENSE	SMC_CPUSA_ISENSE	MAKE_BASE=TRUE	
SMC_CPUDDR_ISENSE	SMC_CPUDDR_ISENSE	MAKE_BASE=TRUE	
SMC_CPUSA_VSENSE	SMC_CPUSA_VSENSE	MAKE_BASE=TRUE	
SMC_CPU_VSENSE	SMC_CPU_VSENSE	MAKE_BASE=TRUE	
SMC_CPUGT_VSENSE	SMC_CPUGT_VSENSE	MAKE_BASE=TRUE	
SMC_CPU_IMON_ISENSE	SMC_CPU_IMON_ISENSE	MAKE_BASE=TRUE	
SMC_CPUGT_IMON_ISENSE	SMC_CPUGT_IMON_ISENSE	MAKE_BASE=TRUE	

SMC12 Pin Assignments

SMC_GFX_PWR_LEVEL_L	SMC_GFX_PWR_LEVEL_L	MAKE_BASE=TRUE
TP_SYS_ONEWIRE	TP_SYS_ONEWIRE	MAKE_BASE=TRUE
TP_SMC_DEBUGPRT_EN_L	TP_SMC_DEBUGPRT_EN_L	MAKE_BASE=TRUE
NC_SMC_DP_HPD_L	NC_SMC_DP_HPD_L	MAKE_BASE=TRUE

PM_THRMTRIP_L

CRITICAL
Q5290
DMN32D2LFB4
DFN1006H4-3
SYM_VER_2

SMC_GFX_OVERTEMP

NC_SPI_SMC_MISO	NC_SPI_SMC_MISO	TRUE	
NC_SPI_SMC_MOSI	NC_SPI_SMC_MOSI	TRUE	
NC_SPI_SMC_CLK	NC_SPI_SMC_CLK	TRUE	
NC_SPI_SMC_CS_L	NC_SPI_SMC_CS_L	TRUE	

SMC_PCH_SUSWARN_L	SMC_PCH_SUSWARN_L	MAKE_BASE=TRUE
SMC_PCH_SUSACK_L	SMC_PCH_SUSACK_L	MAKE_BASE=TRUE
SMC_SENSOR_PWR_EN	SMC_SENSOR_PWR_EN	MAKE_BASE=TRUE
	SMC_SENSOR_PWR_EN	
PM_PWRBTN_L	PM_PWRBTN_L	MAKE_BASE=TRUE
	SMC_BC_ACOK	
SMC_BC_ACOK	SMC_BC_ACOK	MAKE_BASE=TRUE
SMBUS_SMC_4_G3H_SCL	SMBUS_SMC_4_G3H_SCL	MAKE_BASE=TRUE
SMBUS_SMC_4_G3H_SDA	SMBUS_SMC_4_G3H_SDA	MAKE_BASE=TRUE
SMBUS_SMC_2_S4_SCL	SMBUS_SMC_2_S4_SCL	MAKE_BASE=TRUE
SMBUS_SMC_2_S4_SDA	SMBUS_SMC_2_S4_SDA	MAKE_BASE=TRUE
SMC_OOB1_D2R_L	SMC_OOB1_D2R_L	MAKE_BASE=TRUE
SMC_OOB1_R2D_L	SMC_OOB1_R2D_L	MAKE_BASE=TRUE
SMC_ACTUATOR_DISABLE_L	SMC_ACTUATOR_DISABLE_L	MAKE_BASE=TRUE
SMC_CHGR_INT_L	SMC_CHGR_INT_L	MAKE_BASE=TRUE

Debug Power "Buttons"

PLACE_SIDE=TOP
SILK_PART=PWR_BTN
R5226
RES
0603-NSP

BOMOPTION=OMIT

SMC_ONOFF_L

SW5200
EVQPUA02K

BOMOPTION=DBG_BTN
SILK_PART=PWR_BTN
PLACE_SIDE=BOTTOM

Debug RESET "Buttons"

BOMOPTION=DBG_BTN
PLACE_SIDE=BOTTOM
SILK_PART=RESET_BTN
CRITICAL
SW5227
SOX-152HNT
SM

SMC_RESET_L

Hall Effect Pads - Left

J5250
AMR-MLB-X502
SM

HALL_SENSOR_LEFT
PP3V3_G3H

OMIT_TABLE

R5252
10K
5%
1/20W
MF
201

SMC_LID_LEFT_R

C5250
1000PF
10%
16V
X7R-1
0201
NOSTUFF

Hall Effect Pads - Right

J5260
AMR-MLB-X502
SM

HALL_SENSOR_RIGHT
PP3V3_G3H

OMIT_TABLE

R5253
10K
5%
1/20W
MF
201

SMC_LID_RIGHT

C5260
1000PF
10%
16V
X7R-1
0201
NOSTUFF

Thermal Alerts

SMC_CPUHI_COMP_ALERT_L	R5217 100	NOSTUFF	
CPUTHMSNS_THM_L	R5216 100	CPUTHRM_THRM:SMC	
CPUTHMSNS_ALERT_L	R5214 100	CPUTHRM_ALRT:SMC	
TBTTHMSNS_X_THM_L	R5220 100	TBTTHRM_THRM:SMC	
TBTTHMSNS_T_THM_L	R5221 100	TBTTHRM_THRM:SMC	
TBTTHMSNS_X_ALERT_L	R5210 100	TBTTHRM_ALRT:SMC	
TBTTHMSNS_T_ALERT_L	R5211 100	TBTTHRM_ALRT:SMC SMC_SENSOR_ALERT_L	

Specify one of these BOM GROUPs.

BOM GROUP	BOM OPTIONS
CPUTHRM:BOTH	CPUTHRM_THRM:SMC,CPUTHRM_ALRT:SMC
CPUTHRM:THRM	CPUTHRM_THRM:SMC
CPUTHRM:ALRT	CPUTHRM_ALRT:SMC

Specify one of these BOM GROUPs.

BOM GROUP	BOM OPTIONS
TBTTHRM:BOTH	TBTTHRM_THRM:SMC,TBTTHRM_ALRT:SMC
TBTTHRM:THRM	TBTTHRM_THRM:SMC,TBTTHRM_ALRT:PU
TBTTHRM:ALRT	TBTTHRM_THRM:PU,TBTTHRM_ALRT:SMC
TBTTHRM:NONE	TBTTHRM_THRM:PU,TBTTHRM_ALRT:PU

BYPASS=U5256.5::5MM
PP3V3_G3H

R5256
100K
5%
1/20W
MF
201

C5256
0.1UF
10%
10V
X5R-CERM
0201

SMC_LSOC_RST_L
SMC_ONOFF_L

SN74LVC1G02
SOT553-5
U5256
CRITICAL

SMC_4FINGERS_RST

S4 SMC Wake Sources

SMC_PME_S4_WAKE_L	SMC_PME_S4_WAKE_L	MAKE_BASE=TRUE
SMC_PME_S4_DARK_L	SMC_PME_S4_DARK_L	MAKE_BASE=TRUE

R5258
0
5%
1/20W
MF
201
LID_FEATURE_ON

SMC_LID_LEFT

PP3V3_G3H
BYPASS=U5255.6::5MM
C5255
0.1UF
10%
10V
X5R-CERM
0201

R5257
0
5%
1/20W
MF
201
LID_FEATURE_OFF

U5255
74LVC1G32
SOT891

SMC_LID_R
SMC_LID_RIGHT
CRITICAL

R5255
10K
5%
1/20W
MF
201

SMC_LID

R5259
0
5%
1/20W
MF
201

SMC_DEV_SUPPLY_L
SMC_DEV_SUPPLY_R_L

R5260
10
5%
1/20W
MF
201

TCON_BKLT_PWM
BKLT_PWM_TCON2MLB

C5257
3300PF
10%
16V
X7R-CERM
0201
NOSTUFF

NOSTUFF
C5270
1000PF
10%
16V
X7R-CERM
0201

BUF_SMC_RESET_L
GND_SMC_AVSS

BOM_COST_GROUP=SMC

PP3V3_S4

R5274
100K
5%
1/20W
MF
201

R5273
10K
5%
1/20W
MF
201

PLACE_SIDE=BOTTOM
NOSTUFF
R5275
0
5%
1/20W
MF
0201

SMC_DEBUGPRT2_TX_L
WLAN_UART_RX

PLACE_SIDE=BOTTOM
NOSTUFF
R5276
0
5%
1/20W
MF
0201

SMC_DEBUGPRT2_RX_L
WLAN_UART_TX

PP3V3_G3H

R5280
100K
5%
1/20W
MF
201

R5281
10K
5%
1/20W
MF
201

PLACE_SIDE=BOTTOM
R5277
0
5%
1/20W
MF
0201

SMC_DEBUGPRT2_R_TX

TP-P6
TP5200

R5278
0
5%
1/20W
MF
0201
PLACE_SIDE=BOTTOM

SMC_DEBUGPRT2_R_RX

TP-P6
TP5201

SMC_WIFI_PWR_EN	R5295	10K	NOSTUFF
SMC_SENSOR_PWR_EN	R5294	10K	NOSTUFF

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SMC Project Support

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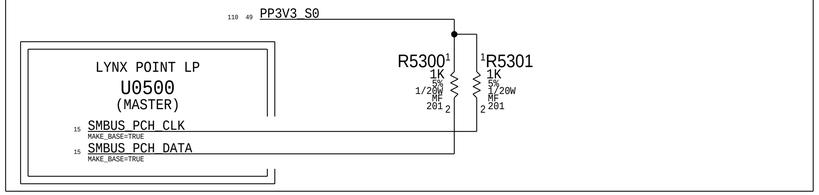
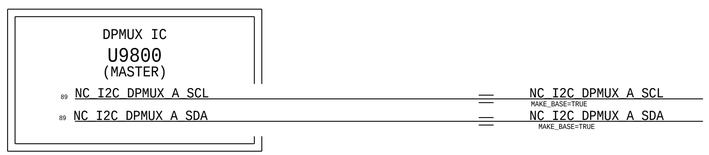
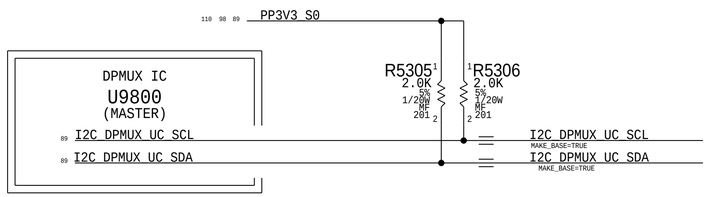
LYNX POINT LP S0 "SMBus 0" Connections



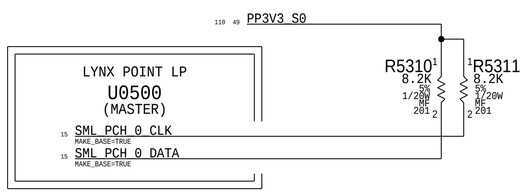
DPMUX Connections



DPMUX Connections



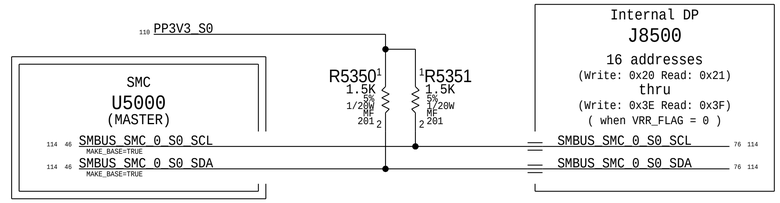
LYNX POINT LP S0 "SMLink 0" Connections



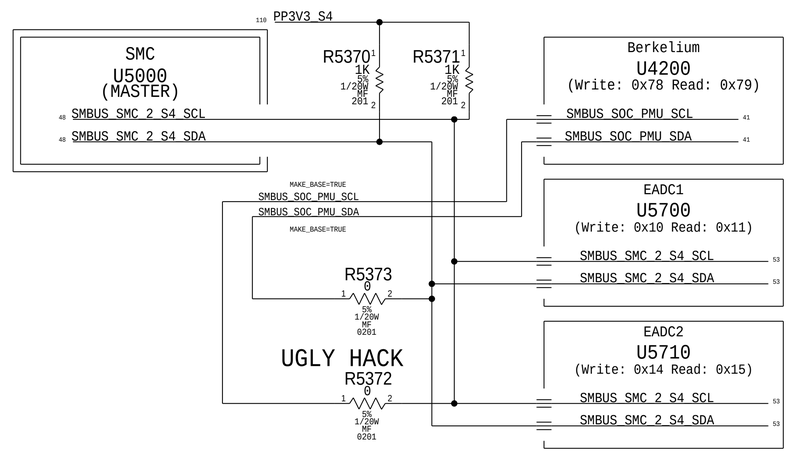
LYNX POINT LP S0 "SMLink 1" Connections

SMLink 1 is slave port to access PCH.

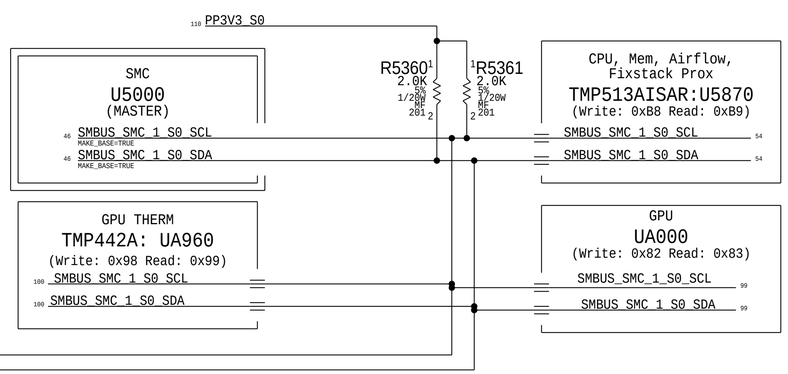
SMC SMBus "0" S0 Connections



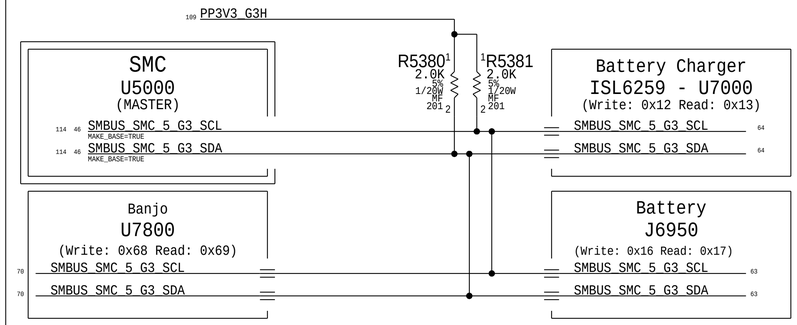
SMC SMBus "2" S4 Connections



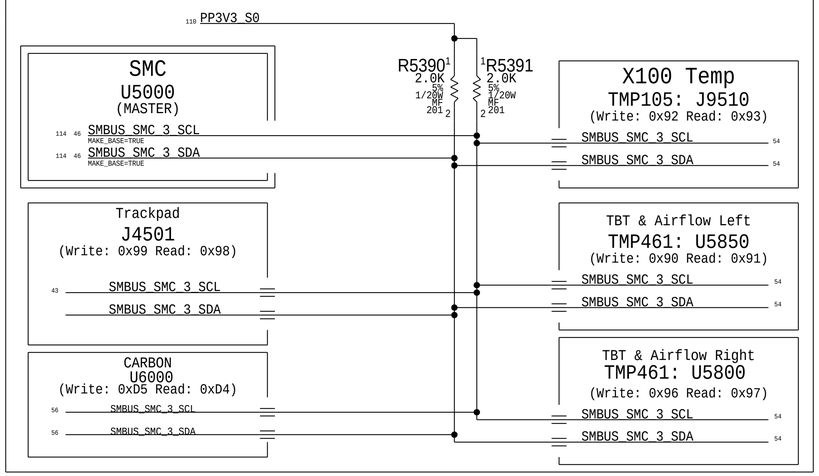
SMC SMBus "1" S0 Connections



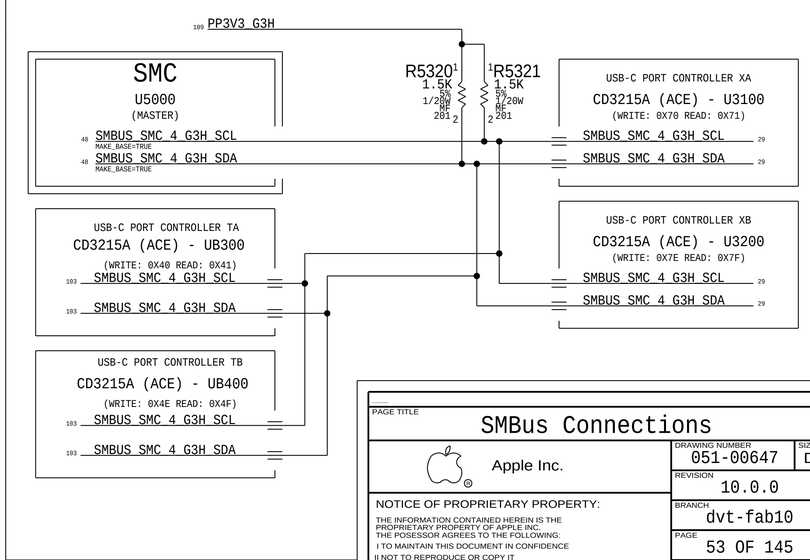
SMC SMBus "5" G3H Connections



SMC SMBus "3" S0 Connections



SMC SMBUS "4" G3H CONNECTIONS



BOM_COST_GROUP=SMC

PAGE TITLE
SMBus Connections

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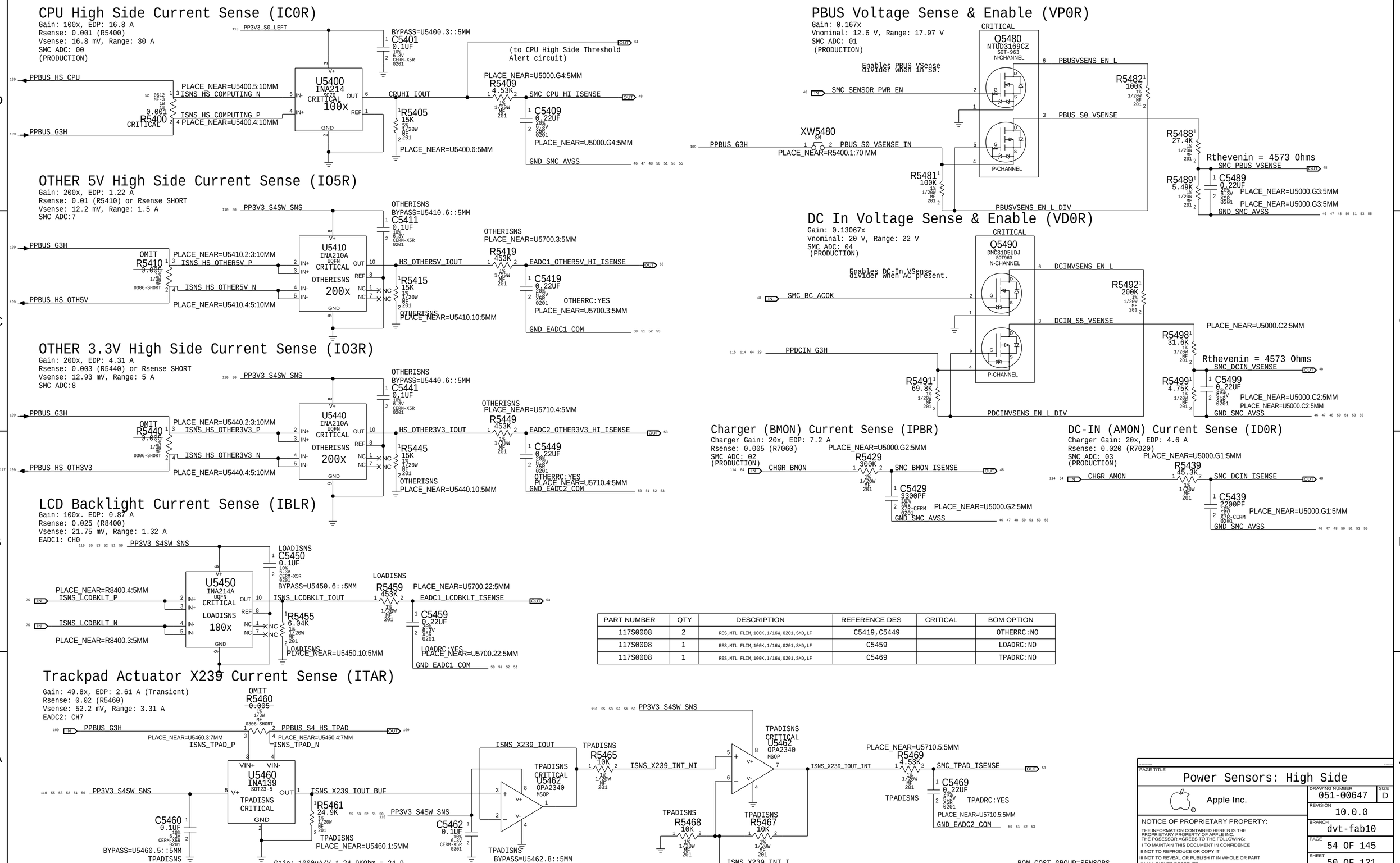

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5419,C5449		OTHERRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5459		LOADRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5469		TPADRC:NO

PAGE TITLE
Power Sensors: High Side

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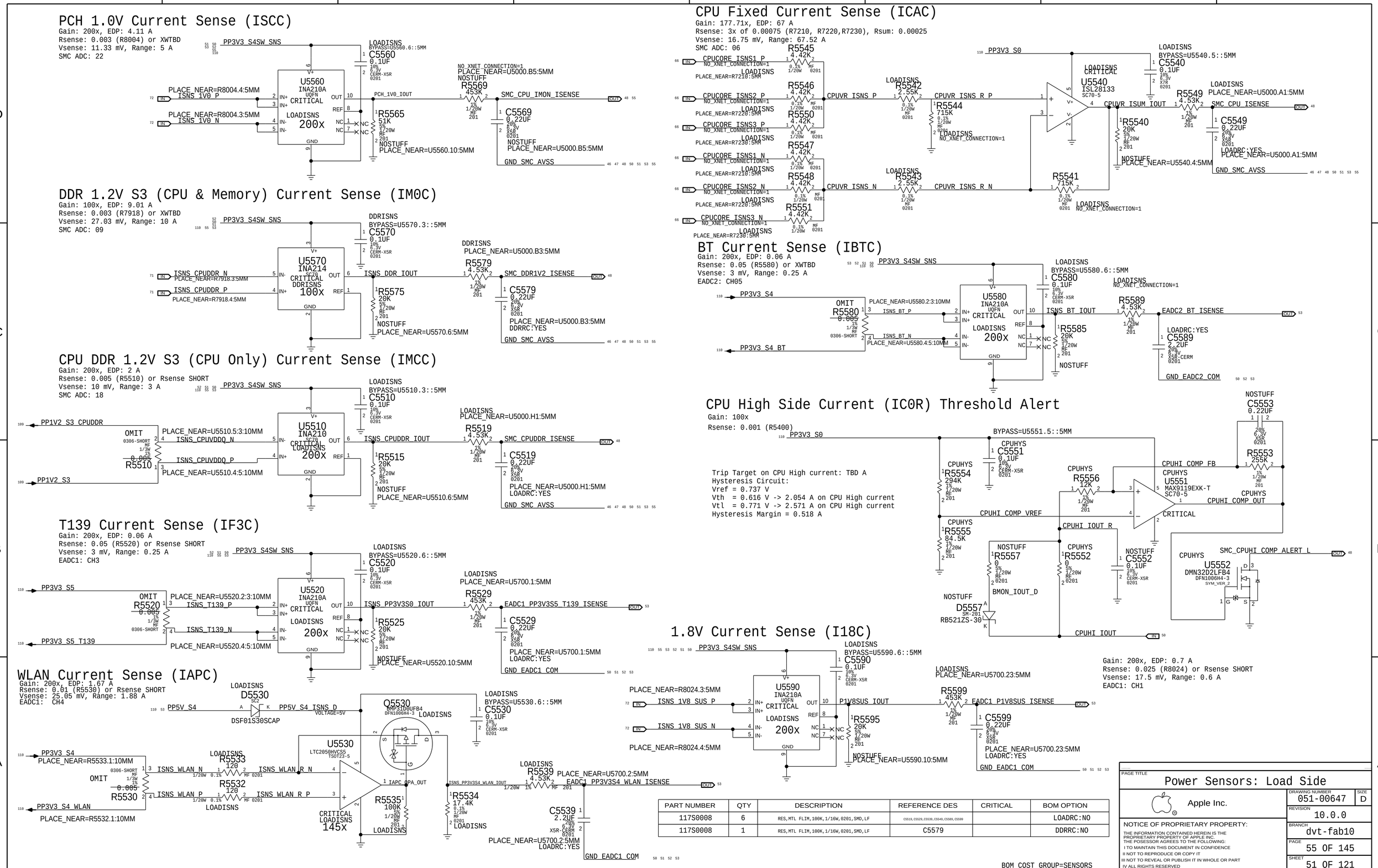

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	6	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5519,C5529,C5539,C5549,C5589,C5599		LOADRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5579		DDRRC:NO

BOM_COST_GROUP=SENSORS

PAGE TITLE
Power Sensors: Load Side

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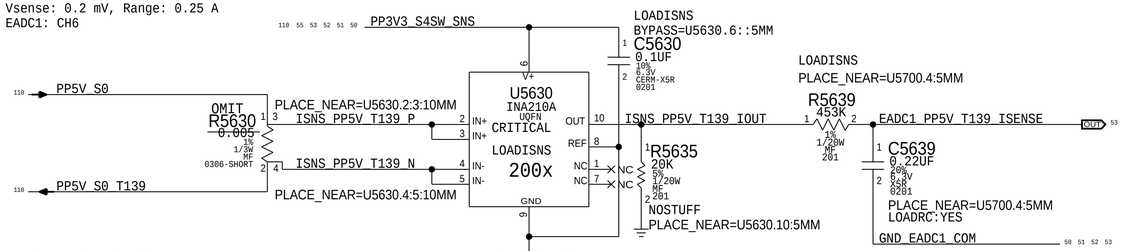
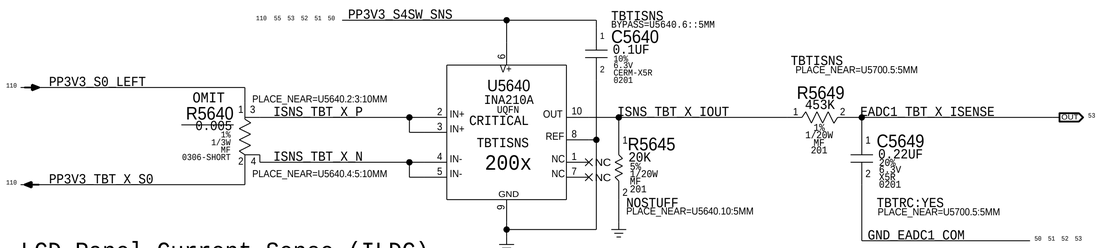
T139 5V Current Sense (IF5C)

Gain: 200x, EDP: 0.004 A
Rsense: 0.05 (R5630) or Rsense SHORT
Vsense: 0.2 mV, Range: 0.25 A
EADC1: CH6



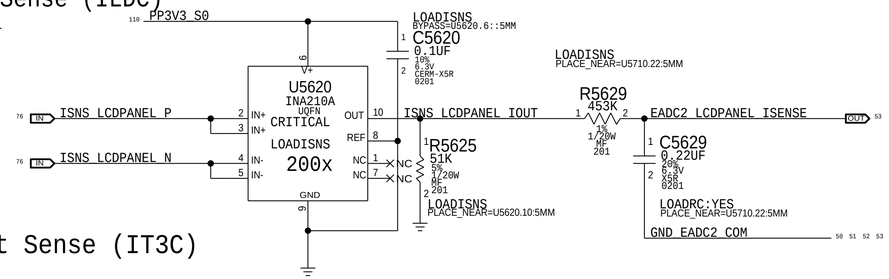
Thunderbolt TBT LEFT Current Sense (IULC)

Gain: 200x. EDP: 0.5 A
Rsense: 0.025 (R5640) or Rsense SHORT
Vsense: 12.5 mV, Range: 0.5 A
EADC1: CH7



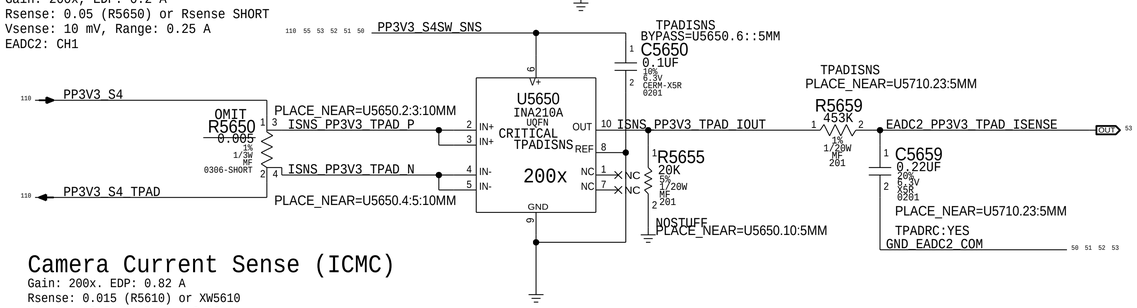
LCD Panel Current Sense (ILDC)

Gain: 200x. EDP: 1 A
RSENSE: 0.01 (R8520) or Rsense SHORT
Vsense: 5 mV, Range: 1.25 A
EADC2: CH0



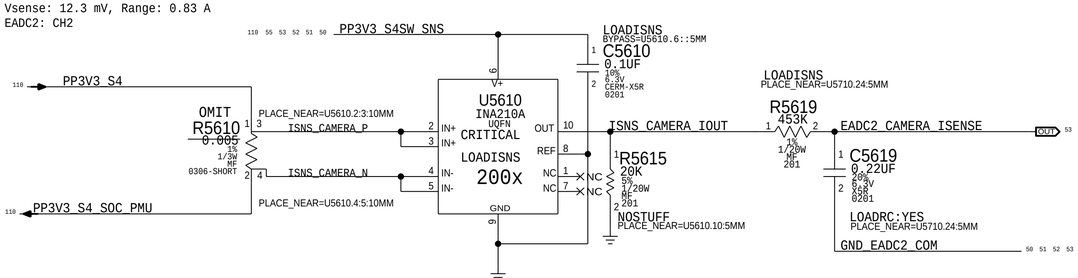
Trackpad 3V Current Sense (IT3C)

Gain: 200x, EDP: 0.2 A
Rsense: 0.05 (R5650) or Rsense SHORT
Vsense: 10 mV, Range: 0.25 A
EADC2: CH1

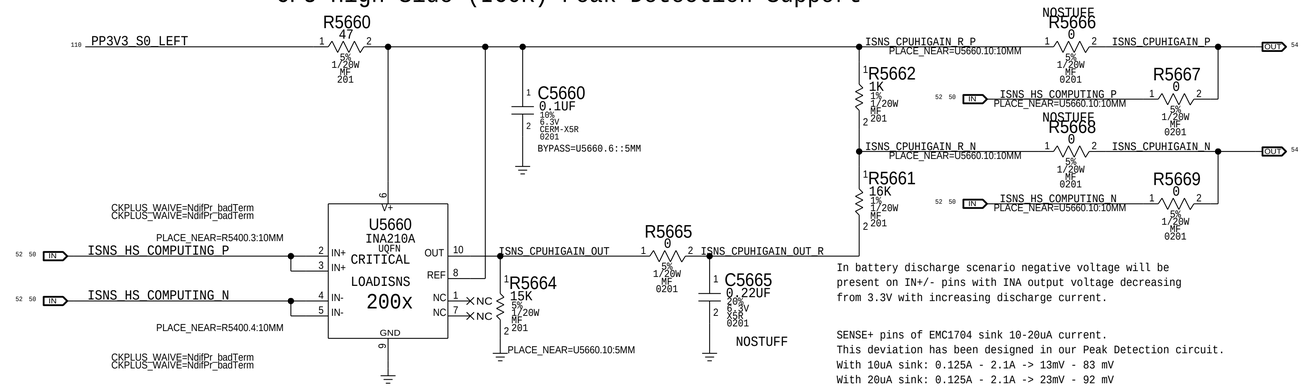


Camera Current Sense (ICMC)

Gain: 200x. EDP: 0.82 A
Rsense: 0.015 (R5610) or XW5610
Vsense: 12.3 mV, Range: 0.83 A
EADC2: CH2



CPU High Side (IC0R) Peak Detection Support

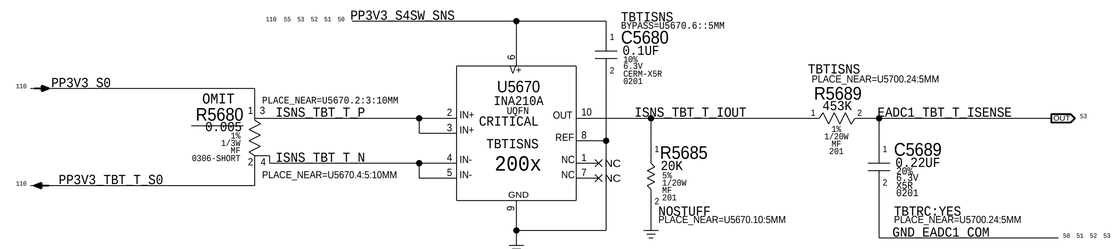


In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

SENSE+ pins of EMC1704 sink 10-20uA current.
This deviation has been designed in our Peak Detection circuit.
With 10uA sink: 0.125A - 2.1A -> 13mV - 83 mV
With 20uA sink: 0.125A - 2.1A -> 23mV - 92 mV

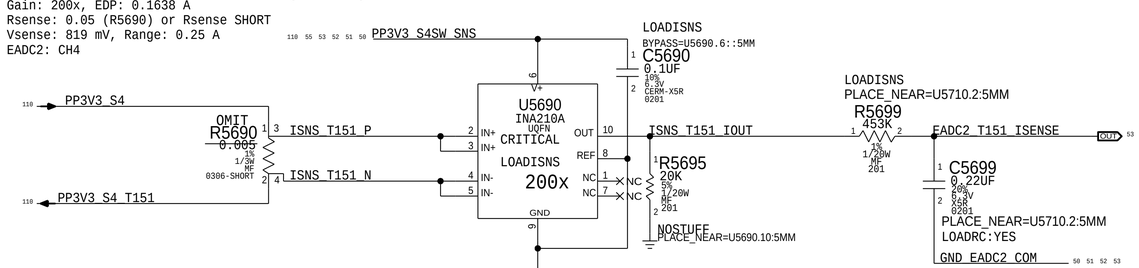
Thunderbolt TBT RIGHT Current Sense (IURC)

Gain: 200x. EDP: 0.5 A
Rsense: 0.025 (R5680) or Rsense SHORT
Vsense: 12.5 mV, Range: 0.5 A
EADC1: CH2



T151 Current Sense (IIDC)

Gain: 200x, EDP: 0.1638 A
Rsense: 0.05 (R5690) or Rsense SHORT
Vsense: 819 mV, Range: 0.25 A
EADC2: CH4



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	4	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5619,C5629,C5639,C5699		LOADRC:NO
117S0008	2	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5649,C5689		TBTRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5659		TPADRC:NO

BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors: Extended

Apple Inc.

DRAWING NUMBER: 051-00647 SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 56 OF 145
SHEET: 52 OF 121

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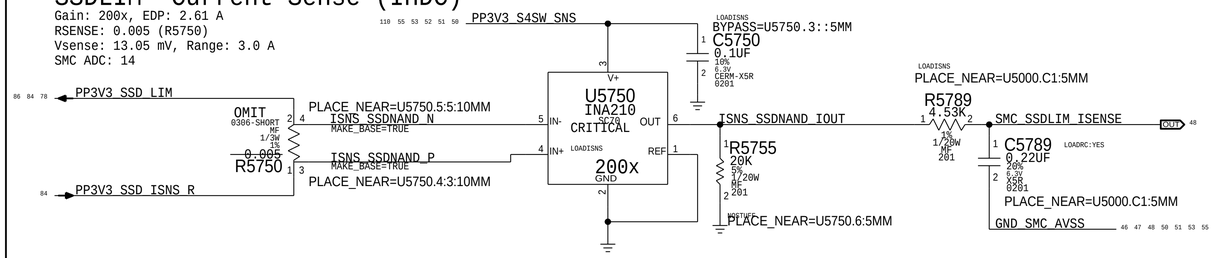
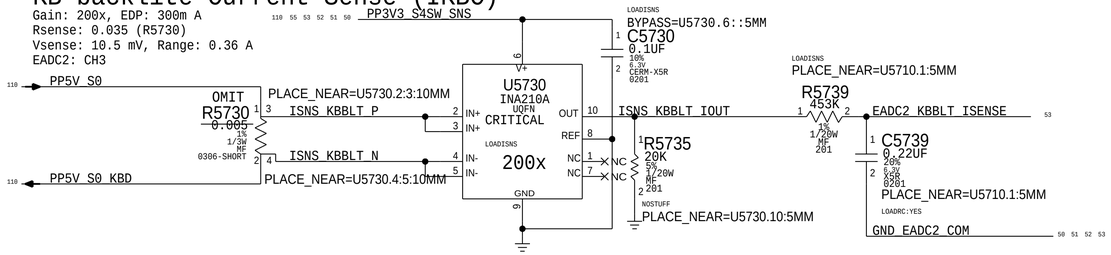
SSDLIM Current Sense (IHDC)

Gain: 200x, EDP: 2.61 A
RSENSE: 0.005 (R5750)
Vsense: 13.05 mV, Range: 3.0 A
SMC ADC: 14



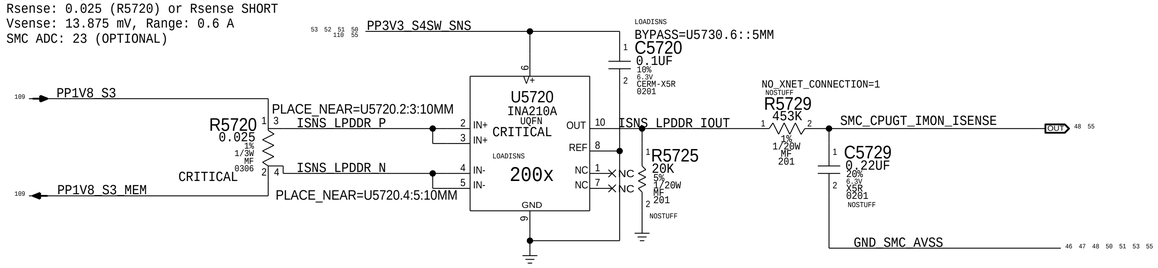
KB backlite Current Sense (IKBC)

Gain: 200x, EDP: 300m A
Rsense: 0.035 (R5730)
Vsense: 10.5 mV, Range: 0.36 A
EADC2: CH3



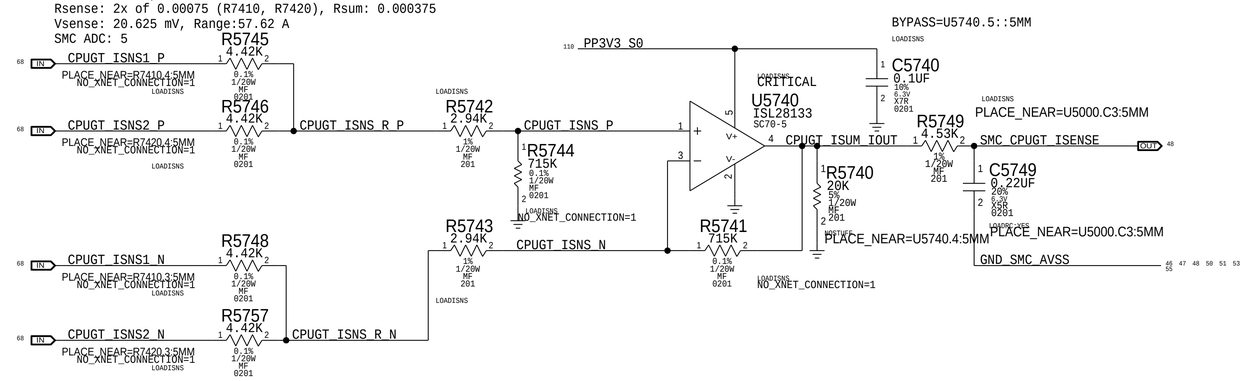
LPDDR 1.8V Current Sense (IM1C)

Gain: 200x, EDP: 0.555 A
Rsense: 0.025 (R5720) or Rsense SHORT
Vsense: 13.875 mV, Range: 0.6 A
SMC ADC: 23 (OPTIONAL)



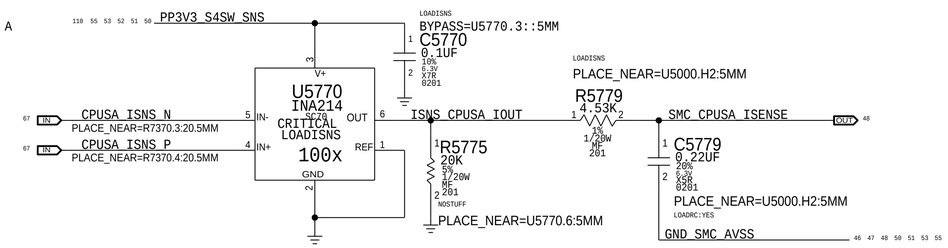
CPU GT Current Sense (ICTC)

Gain: 202.93x, EDP: 55 A
Rsense: 2x of 0.00075 (R7410, R7420), Rsum: 0.000375
Vsense: 20.625 mV, Range:57.62 A
SMC ADC: 5



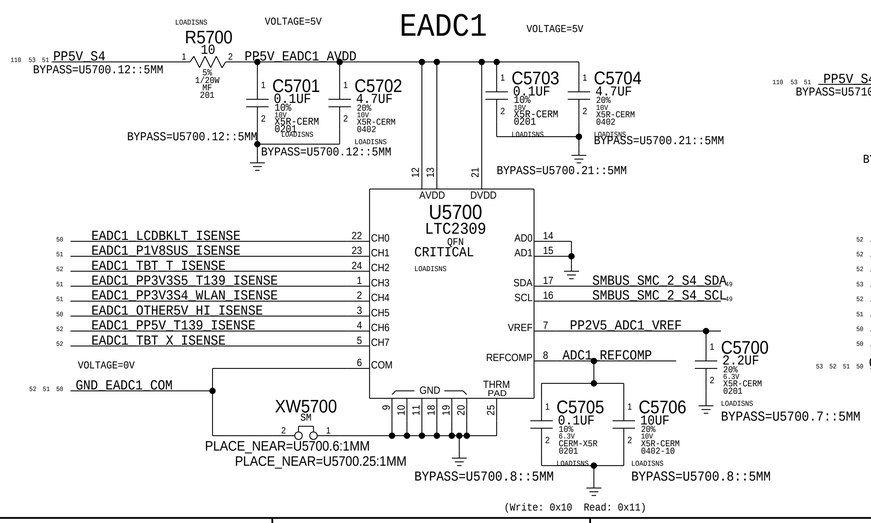
CPU SA Current Sense (ICSC)

Gain: 200x, EDP: 8 A
Rsense: 0.002 (R7570)
Vsense: 16 mV, Range: 7.5 A
SMC ADC: 17

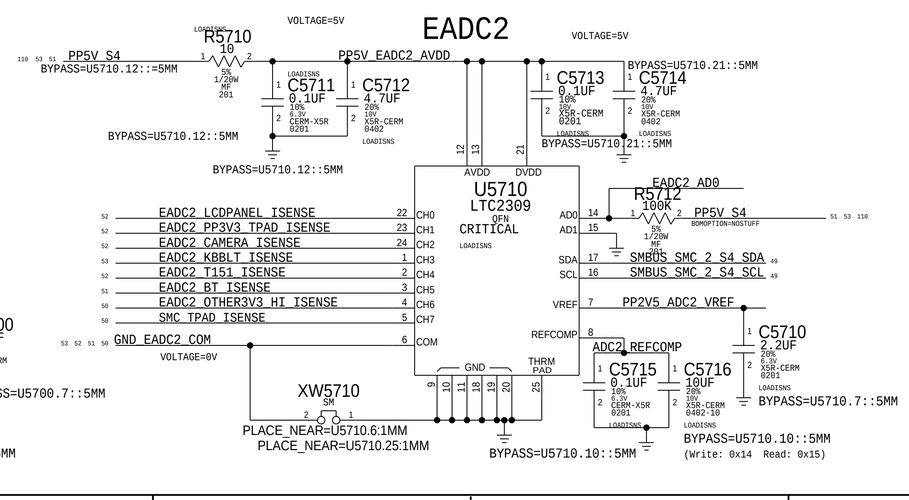


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	4	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5739,C5749,C5779,C5789		LOADRC:NO

EADC1

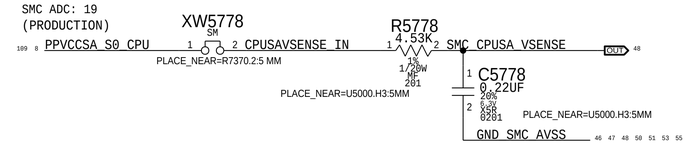


EADC2



CPU SA Voltage Sense (VCSC)

SMC ADC: 19
(PRODUCTION)



BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors: Extended 2

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DRAWING NUMBER: 051-00647 | SIZE: D
REVISION: 10.0.0
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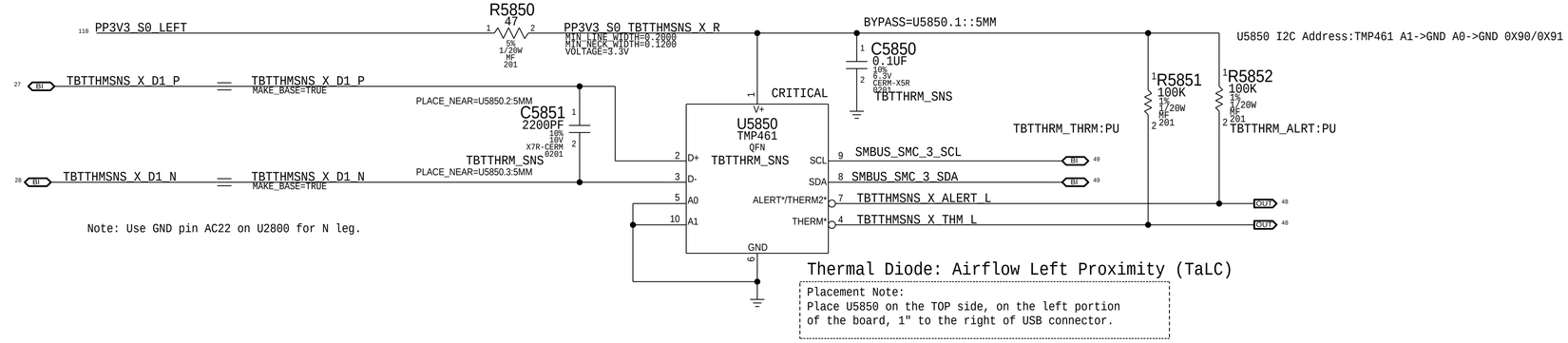
Thermal Sensor A: Thunderbolt Die, Airflow Left

I2C Write: 0xD8, I2C Read: 0xD9

Thermal Diode: TBT Die (TTLD)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.



Thermal Diode: Airflow Left Proximity (TaLC)

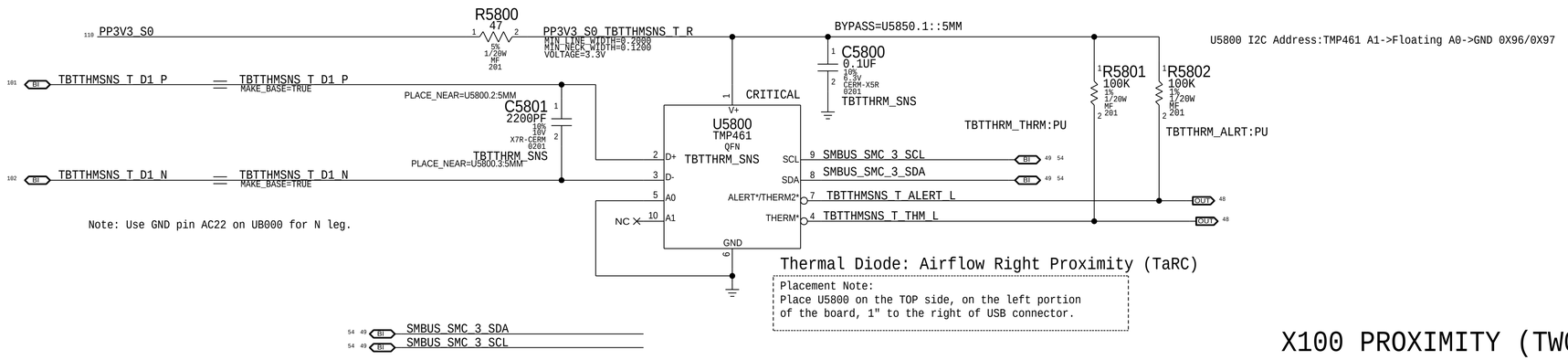
Placement Note:
Place U5850 on the TOP side, on the left portion of the board, 1" to the right of USB connector.

Thermal Sensor C: Thunderbolt Die, Air Flow Right

I2C Write: 0x98, I2C Read: 0x99

Thermal Diode: TBT Die (TTRD)

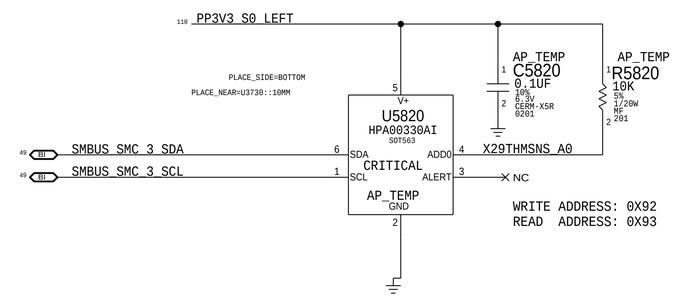
Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.



Thermal Diode: Airflow Right Proximity (TaRC)

Placement Note:
Place U5800 on the TOP side, on the left portion of the board, 1" to the right of USB connector.

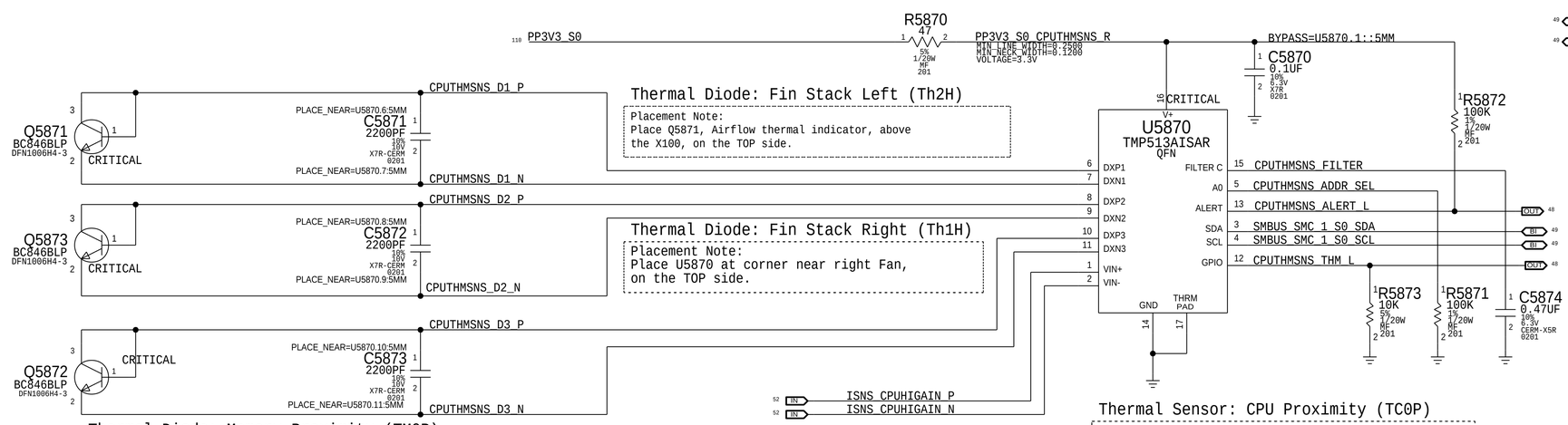
X100 PROXIMITY (TW0P)



Placement note:
PLACE U5820 ON BOTTOM NEAR X100

Thermal Sensor B & CPU High Peak Detection: CPU Proximity, Memory Proximity, Fin Stack Left, Fin Stack Right

I2C Write: 0x98, I2C Read: 0x99



Thermal Diode: Fin Stack Left (Th2H)

Placement Note:
Place Q5871, Airflow thermal indicator, above the X100, on the TOP side.

Thermal Diode: Fin Stack Right (Th1H)

Placement Note:
Place U5870 at corner near right Fan, on the TOP side.

Thermal Diode: Memory Proximity (TM0P)

Placement Note:
Place Q5872 between two rows of Memory devices, between channel A and B, on the BOTTOM side.

Thermal Sensor: CPU Proximity (TC0P)

Placement Note:
Place Q5873 under the CPU, on the BOTTOM side.

I2C ADDRESS (U5870): 0XB8/0XB9

BOM_COST_GROUP=SENSORS

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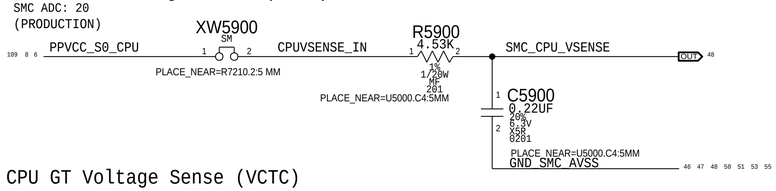
SENSORS: EXTENDER 3

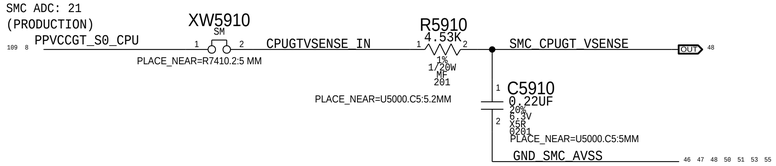
CPU Core Voltage Sense (VCAC)

SMC ADC: 20
(PRODUCTION)



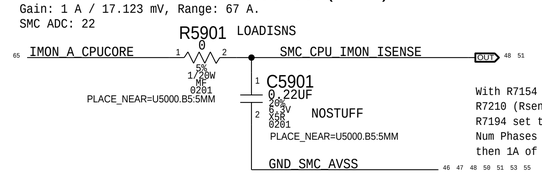
CPU GT Voltage Sense (VCTC)

SMC ADC: 21
(PRODUCTION)



CPU Core IMON Current Sense (ICAM)

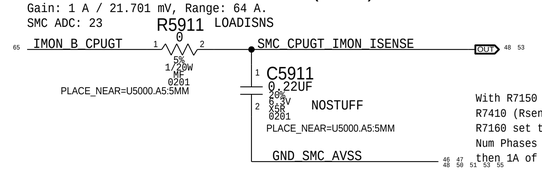
Gain: 1 A / 17.123 mV, Range: 67 A.
SMC ADC: 22



With R7154 (Ri) set to 365 Ohm,
R7210 (Rsen) set to 0.75 mOhm,
R7194 set to 100 kOhm,
Num Phases (N) is 3, and Io (ICCmax) is 67A,
then 1A of Io gives 17.123mV at the Vimon.

CPU GT IMON Current Sense (ICTM)

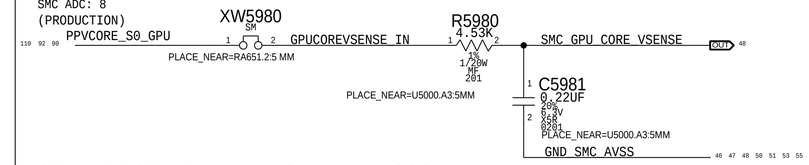
Gain: 1 A / 21.701 mV, Range: 64 A.
SMC ADC: 23



With R7150 (Ri) set to 432 Ohm,
R7410 (Rsen) set to 0.75 mOhm,
R7160 set to 100 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 55A,
then 1A of Io gives 21.701mV at the Vimon.

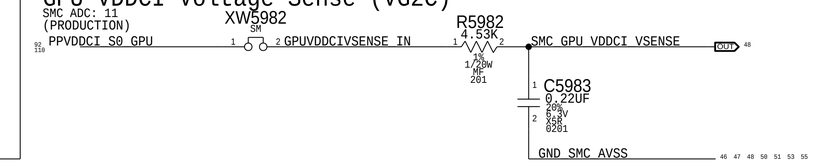
GPU CORE Voltage Sense (VG0C)

SMC ADC: 8
(PRODUCTION)



GPU VDDCI Voltage Sense (VG2C)

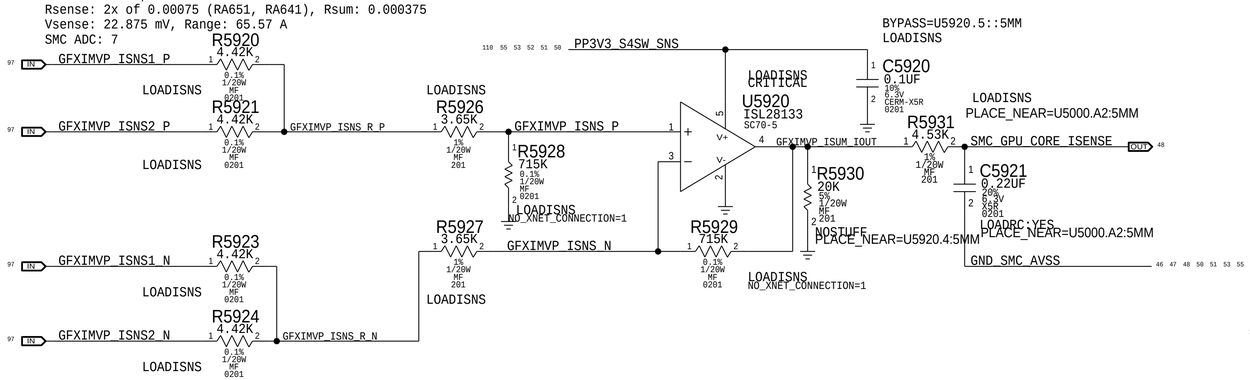
SMC ADC: 11
(PRODUCTION)



GPU SENSORS

GPU CORE Current Sense (IG0C)

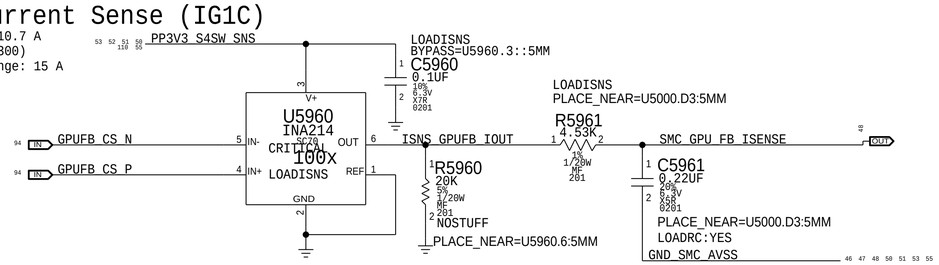
Gain: 122.01x, EDP: 64.2 A
Rsense: 2x of 0.00075 (RA651, RA641), Rsum: 0.000375
Vsense: 22.875 mV, Range: 65.57 A
SMC ADC: 7



BYPASS=U5920.5::5MM
LOADISNS

GPU FB Current Sense (IG1C)

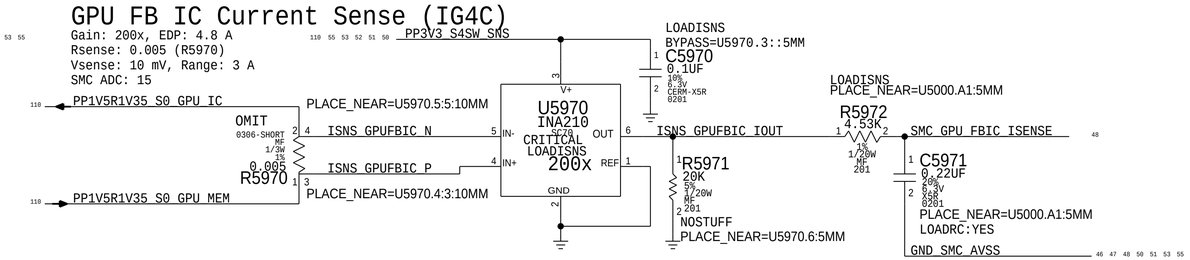
Gain: 100x, EDP: 10.7 A
Rsense: 0.002 (RA300)
Vsense: 16 mV, Range: 15 A
SMC ADC: 13



LOADISNS
BYPASS=U5960.3::5MM
LOADISNS
PLACE_NEAR=U5000.D3:5MM

GPU FB IC Current Sense (IG4C)

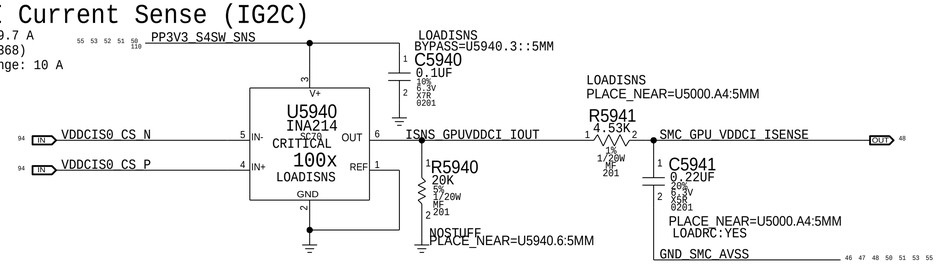
Gain: 200x, EDP: 4.8 A
Rsense: 0.005 (R5970)
Vsense: 10 mV, Range: 3 A
SMC ADC: 15



LOADISNS
BYPASS=U5970.3::5MM
LOADISNS
PLACE_NEAR=U5000.A1:5MM

GPU VDDCI Current Sense (IG2C)

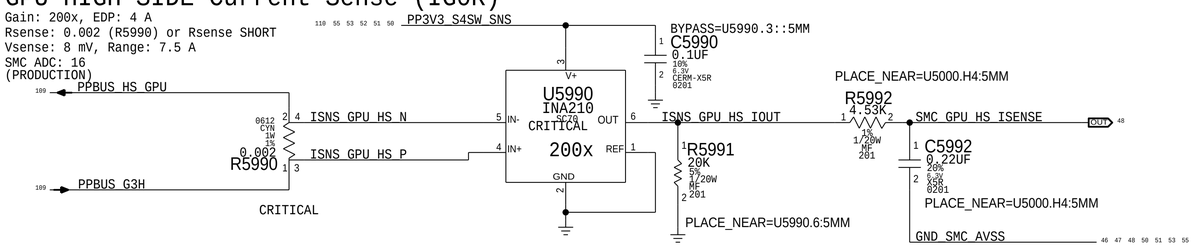
Gain: 100x, EDP: 9.7 A
Rsense: 0.003 (RA368)
Vsense: 24 mV, Range: 10 A
SMC ADC: 10



LOADISNS
BYPASS=U5940.3::5MM
LOADISNS
PLACE_NEAR=U5000.A4:5MM

GPU HIGH SIDE Current Sense (IG0R)

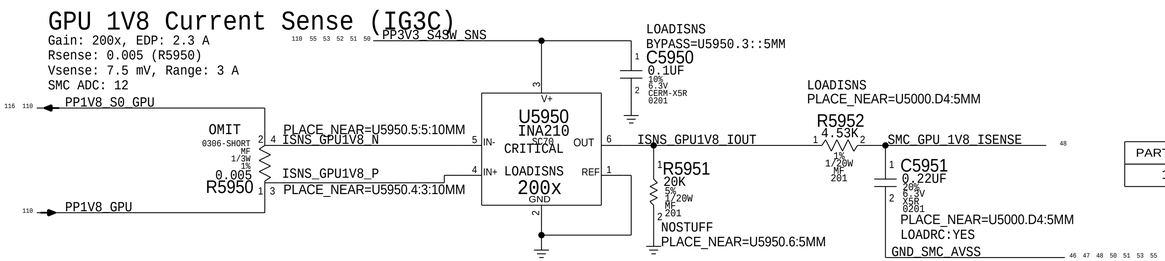
Gain: 200x, EDP: 4 A
Rsense: 0.002 (R5990) or Rsense SHORT
Vsense: 8 mV, Range: 7.5 A
SMC ADC: 16
(PRODUCTION)



BYPASS=U5990.3::5MM
PLACE_NEAR=U5000.H4:5MM
CRITICAL

GPU 1V8 Current Sense (IG3C)

Gain: 200x, EDP: 2.3 A
Rsense: 0.005 (R5950)
Vsense: 7.5 mV, Range: 3 A
SMC ADC: 12



LOADISNS
BYPASS=U5950.3::5MM
LOADISNS
PLACE_NEAR=U5000.D4:5MM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	5	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5921,C5941,C5951,C5961,C5971		LOADRC:NO

BOM_COST_GROUP=SENSORS

PAGE TITLE
Sensor Extended 3

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DRAWING NUMBER 051-00647
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REVISION 10.0.0
BRANCH dvt-fab10
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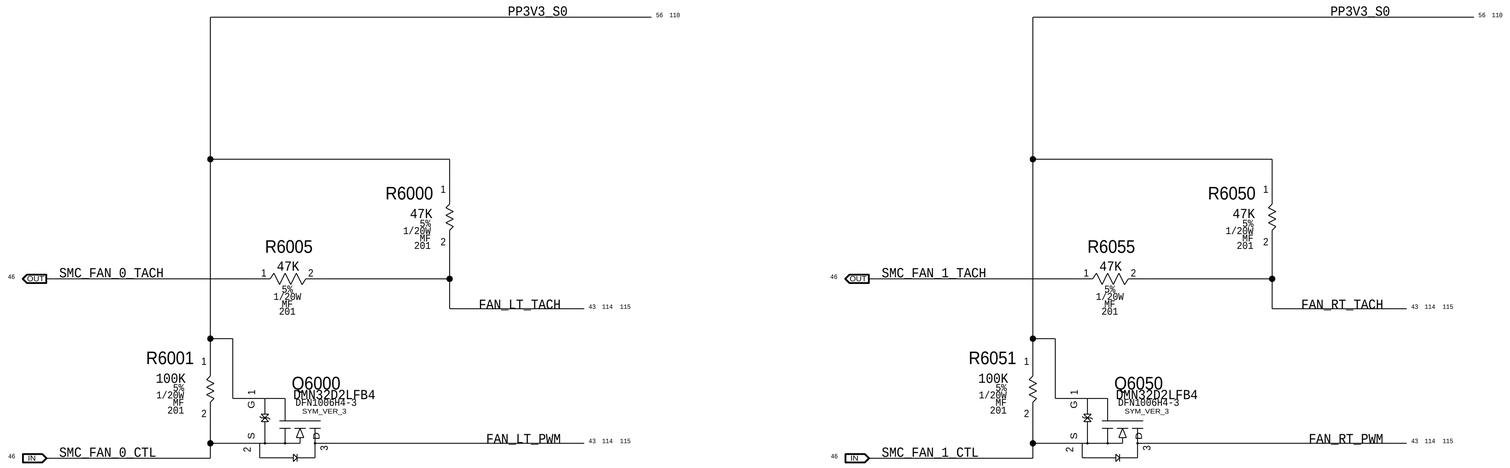
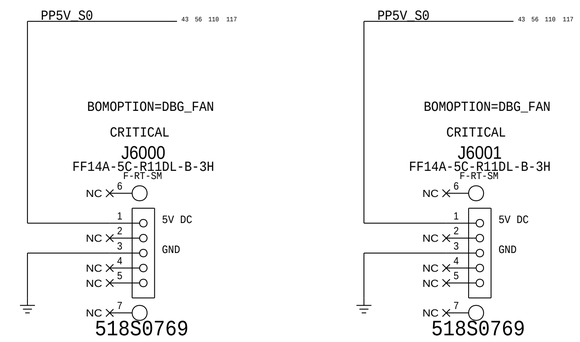
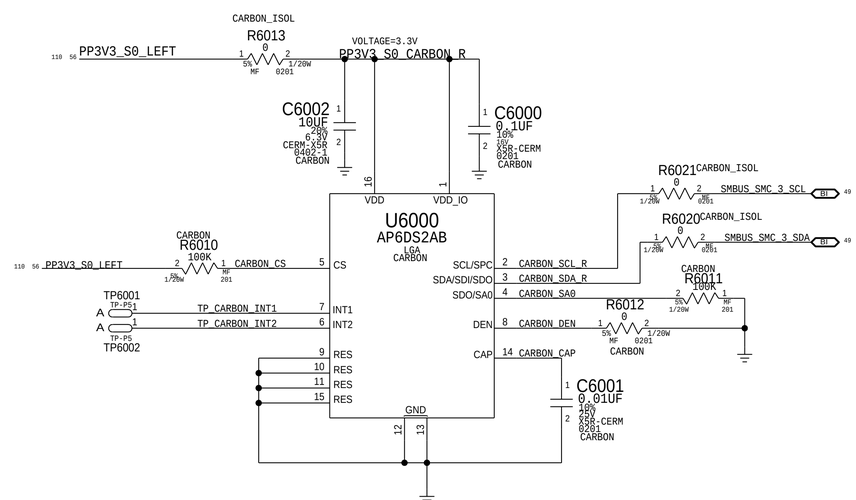
FAN CONNECTOR

KEEP THE 5 PIN CONNECTOR FROM D1







BOM_COST_GROUP=FAN

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Apple Inc.	DRAWING NUMBER 051-00647 · SIZE D
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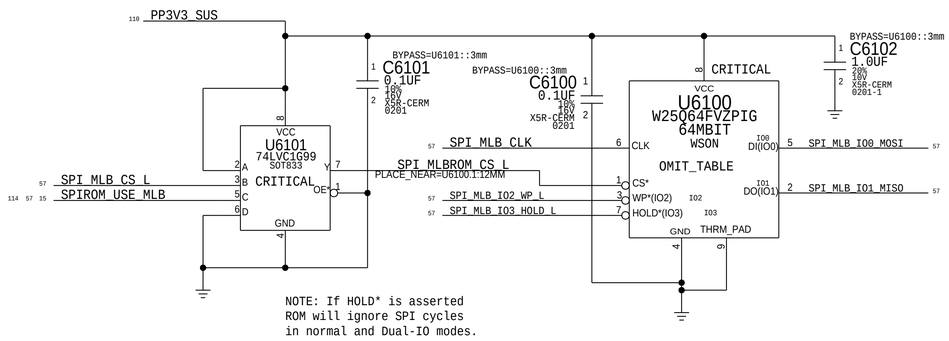
SPI ROM

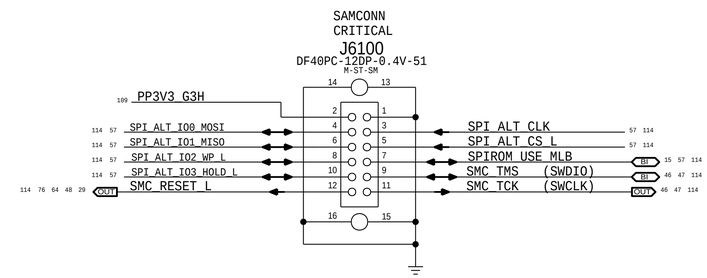
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



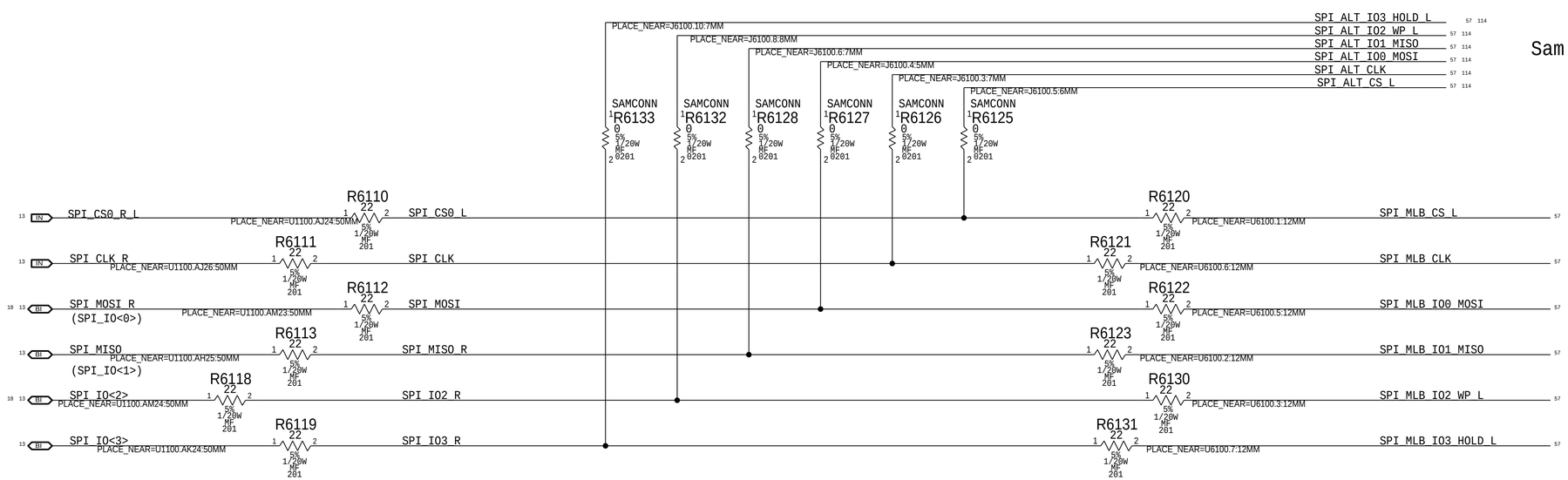
NOTE: If HOLD* is asserted
ROM will ignore SPI cycles
in normal and Dual-IO modes.

Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE)
in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

SPI+SWD SAM Connector



SPI Bus Series Termination (Modified per PDG)



BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE
SPI Debug Connector

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 61 OF 145
SHEET 57 OF 121

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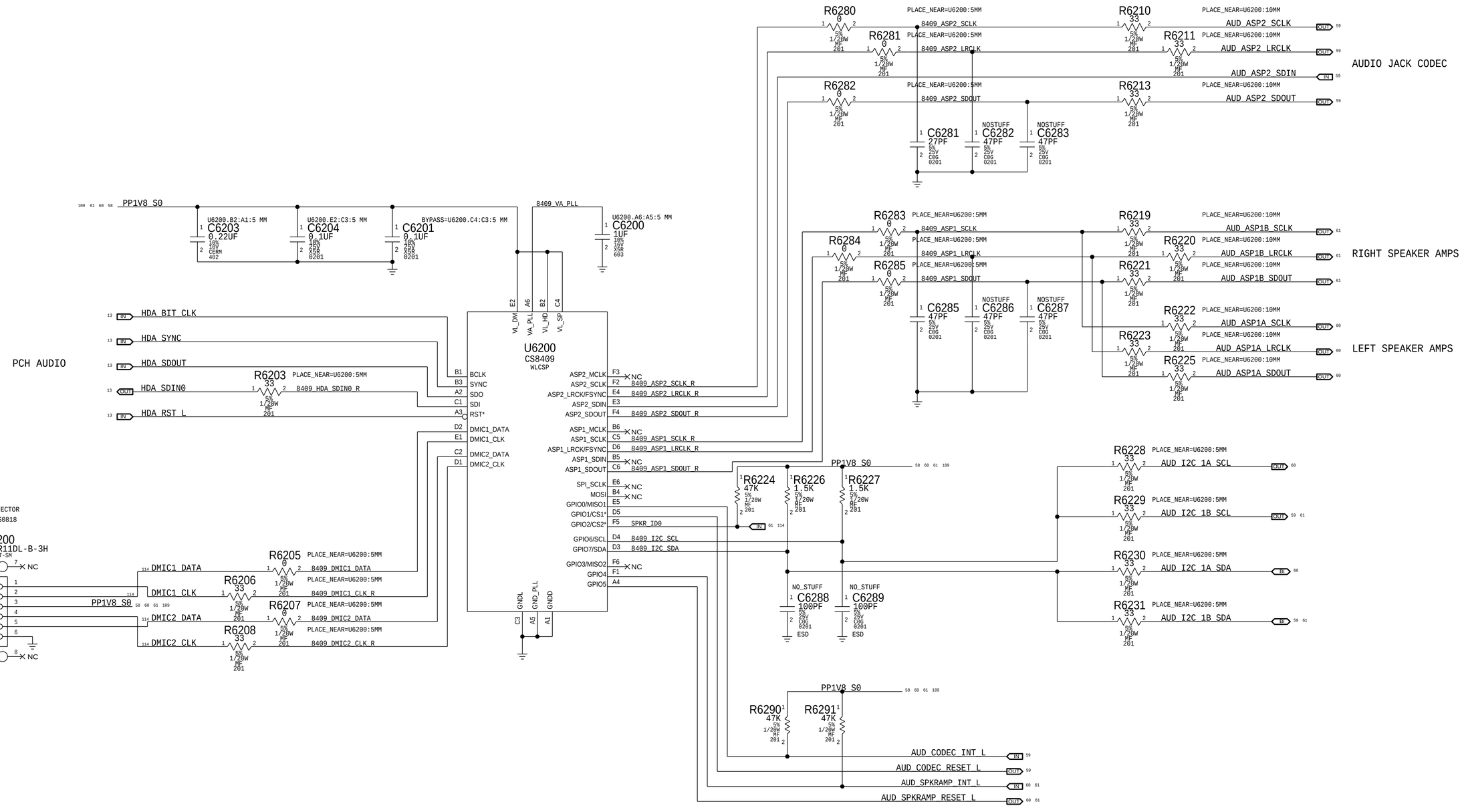

BOM_COST_GROUP=AUDIO

PAGE TITLE	HDA Bridge
Apple Inc.	DRAWING NUMBER 051-00647 SIZE D
	REVISION 10.0.0
	BRANCH dvt-fab10
	PAGE 62 OF 145
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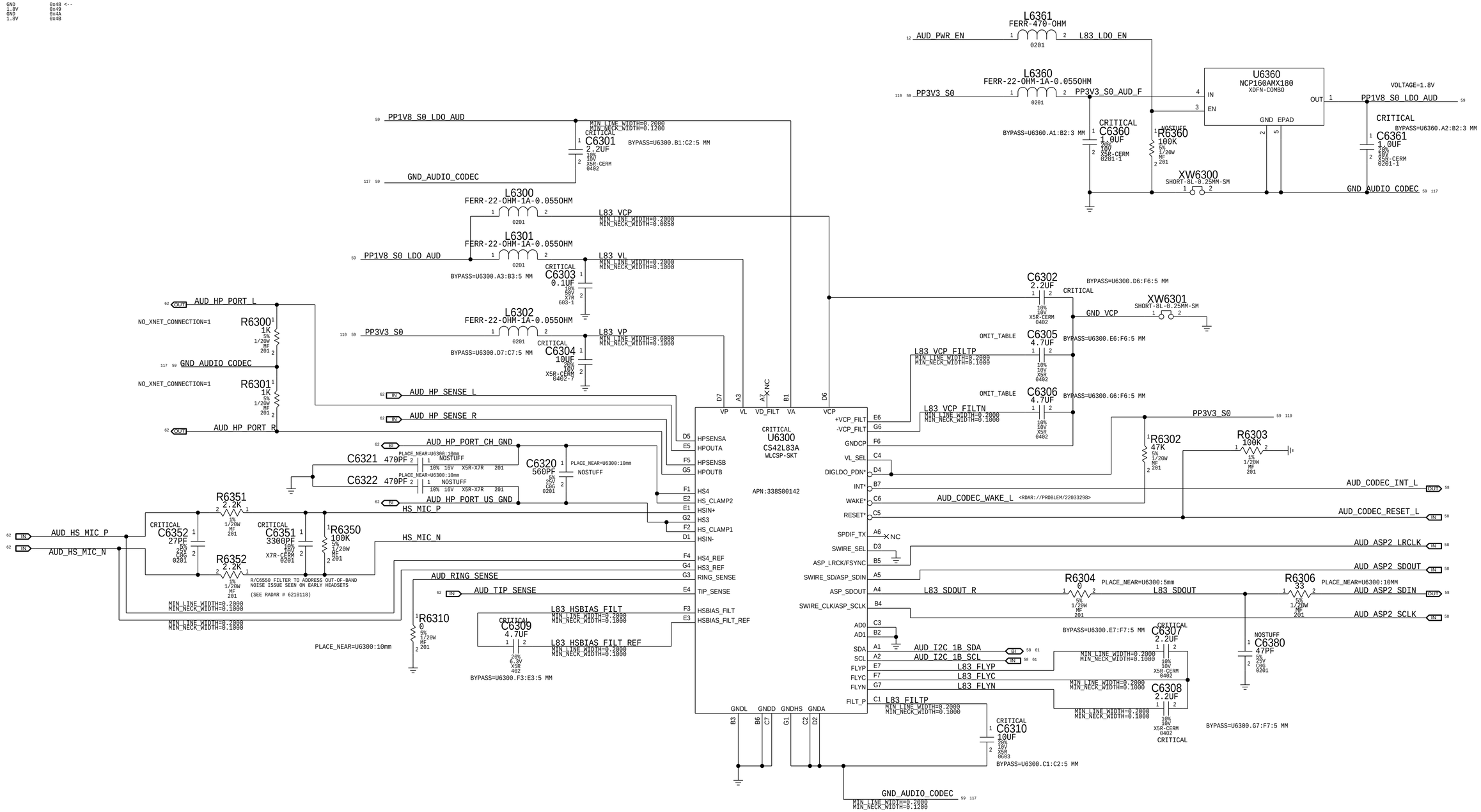
AUDIO JACK CODEC I2C ADDRESS

AD1	AD0	ADDRESS
GND	GND	0x48 <--
GND	1.8V	0x49
1.8V	GND	0x4A
1.8V	1.8V	0x4B



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0719	2	CAP,CER,4.7UF,20%,10V,X5R,0402,MURATA	C6305,C6306	CRITICAL	

PAGE TITLE

AUDIO JACK CODEC

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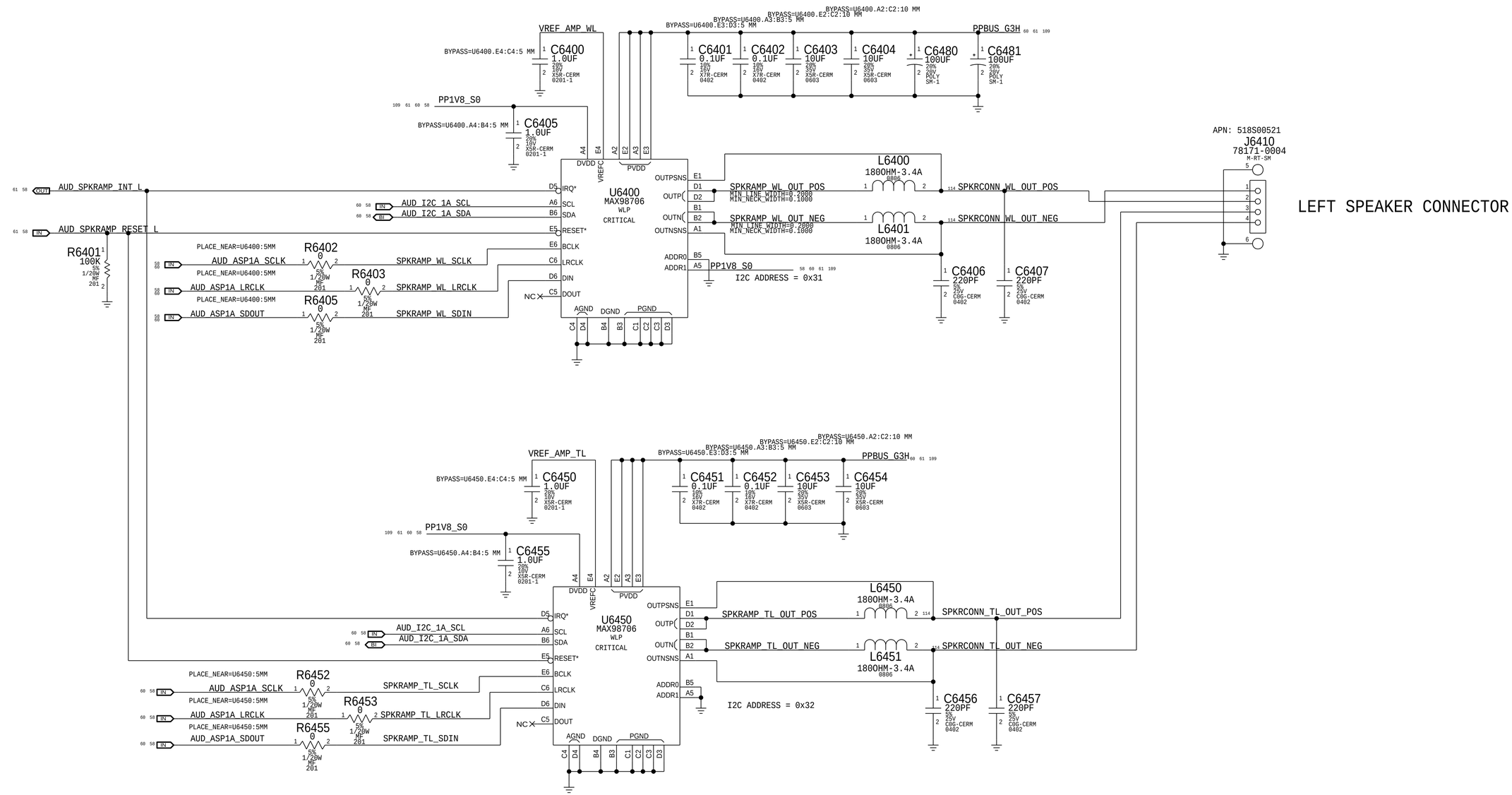
2X MONO SPEAKER AMPLIFIER
APN: 353S00604
0dBFS = 9VPK



BOM_COST_GROUP=AUDIO

PAGE TITLE
AUDIO Speaker Amps & Conn

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 64 OF 145
SHEET 60 OF 121

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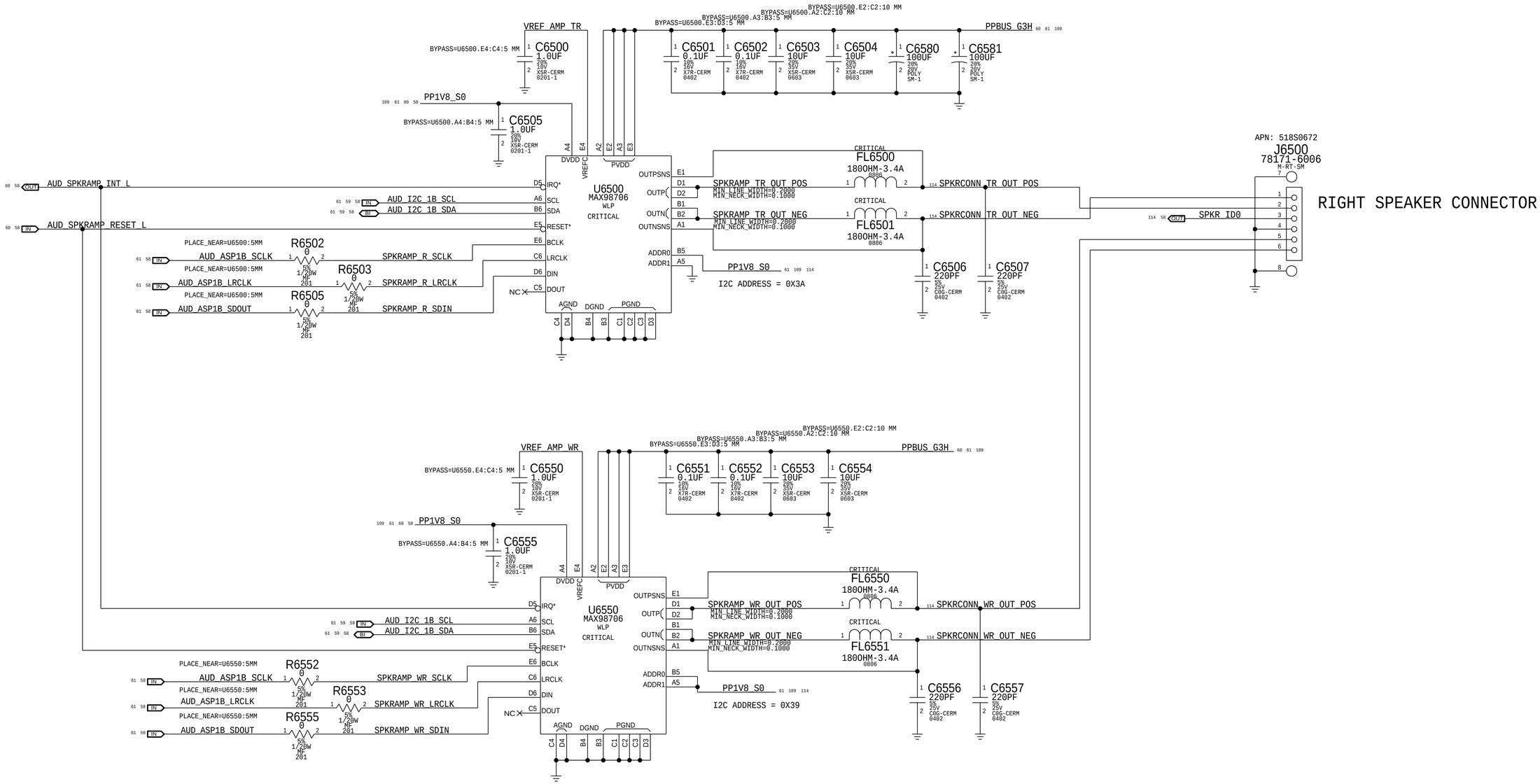
2X MONO SPEAKER AMPLIFIER
APN: 353S00604
0dBFS = 9VPK



BOM_COST_GROUP=AUDIO

PAGE TITLE
AUDIO Speaker Amps & Conn

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BRANCH dvt-fab10
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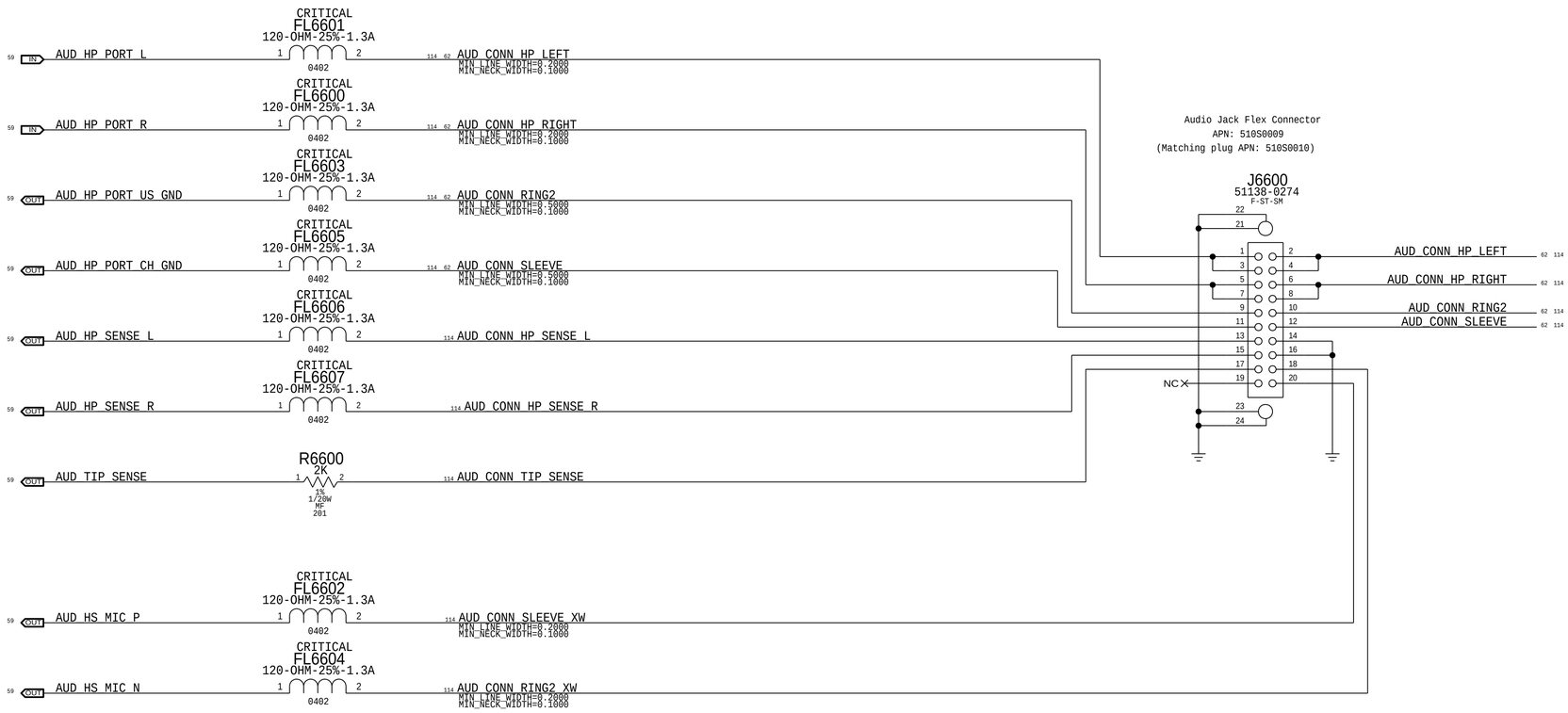

BOM_COST_GROUP=AUDIO

PAGE TITLE

AUDIO JACK CONNECTOR

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SHEET 62 OF 121

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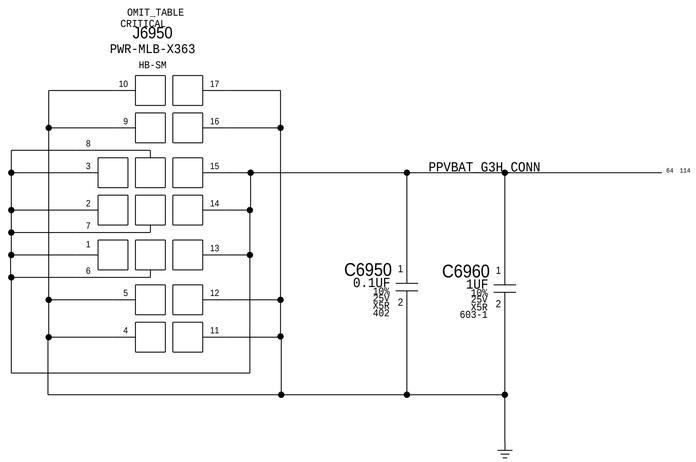
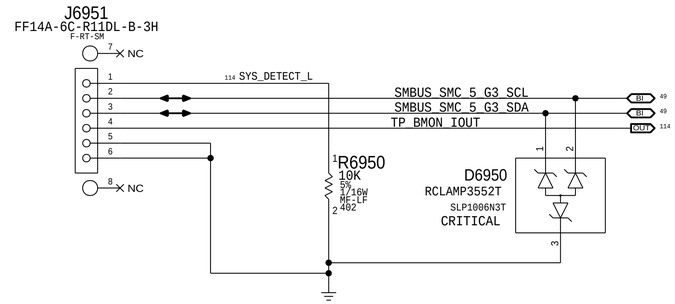
J80 Battery Hotbar Flex Pads 998-03902
Flex Pad TO MLB 998-03780.

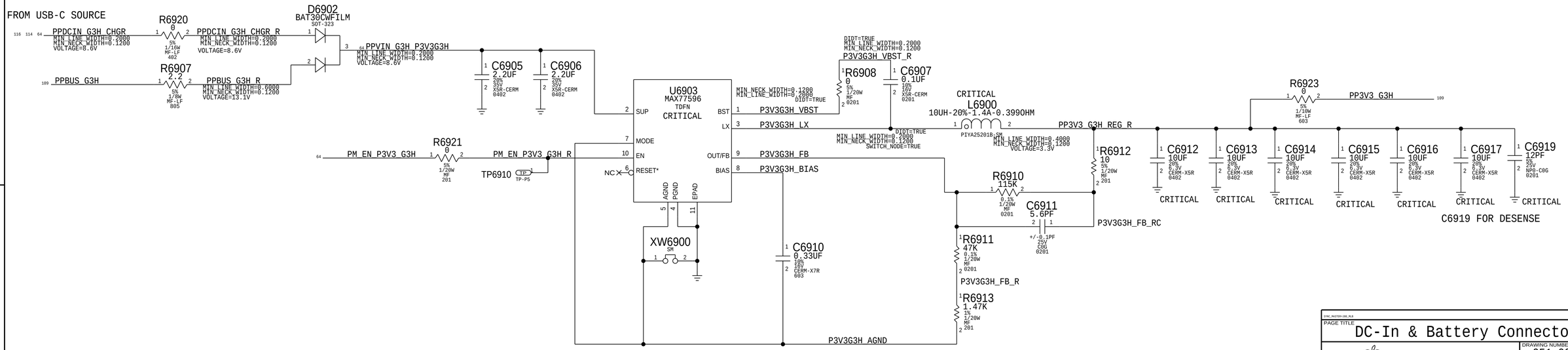
APN:518S0818





BMU POWER FLEX HOTBAR'd TO THE MLB:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-00862	1	PCBA,FLEX,BMU PWR,X363	J6950	CRITICAL	



BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 69 OF 145
SHEET 63 OF 121

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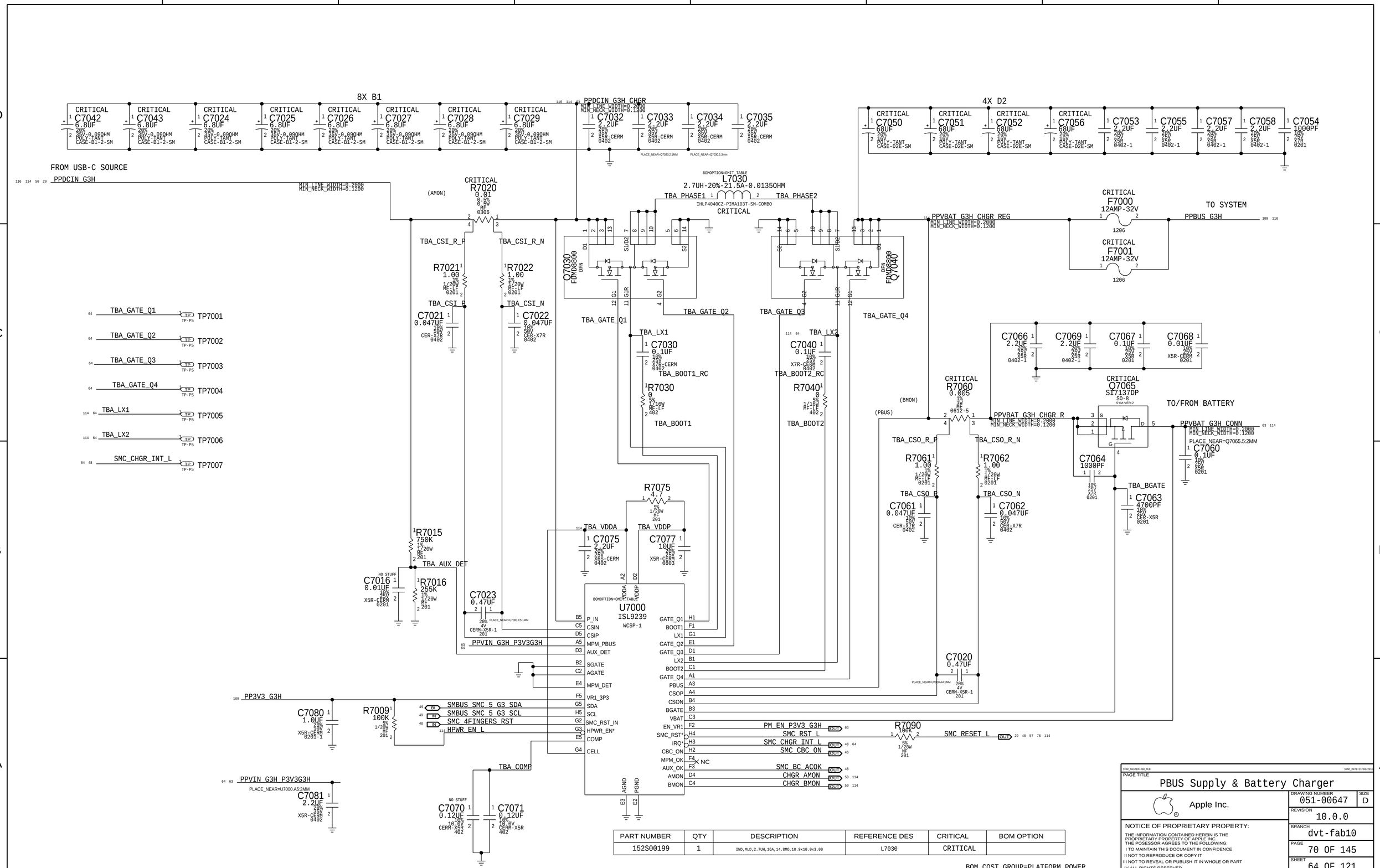

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00199	1	IND,MLD,2.7UH,16A,14.8MO,10.9x10.0x3.00	L7030	CRITICAL	

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
PBUS Supply & Battery Charger

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D
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BRANCH dvt-fab10
PAGE 70 OF 145
SHEET 64 OF 121

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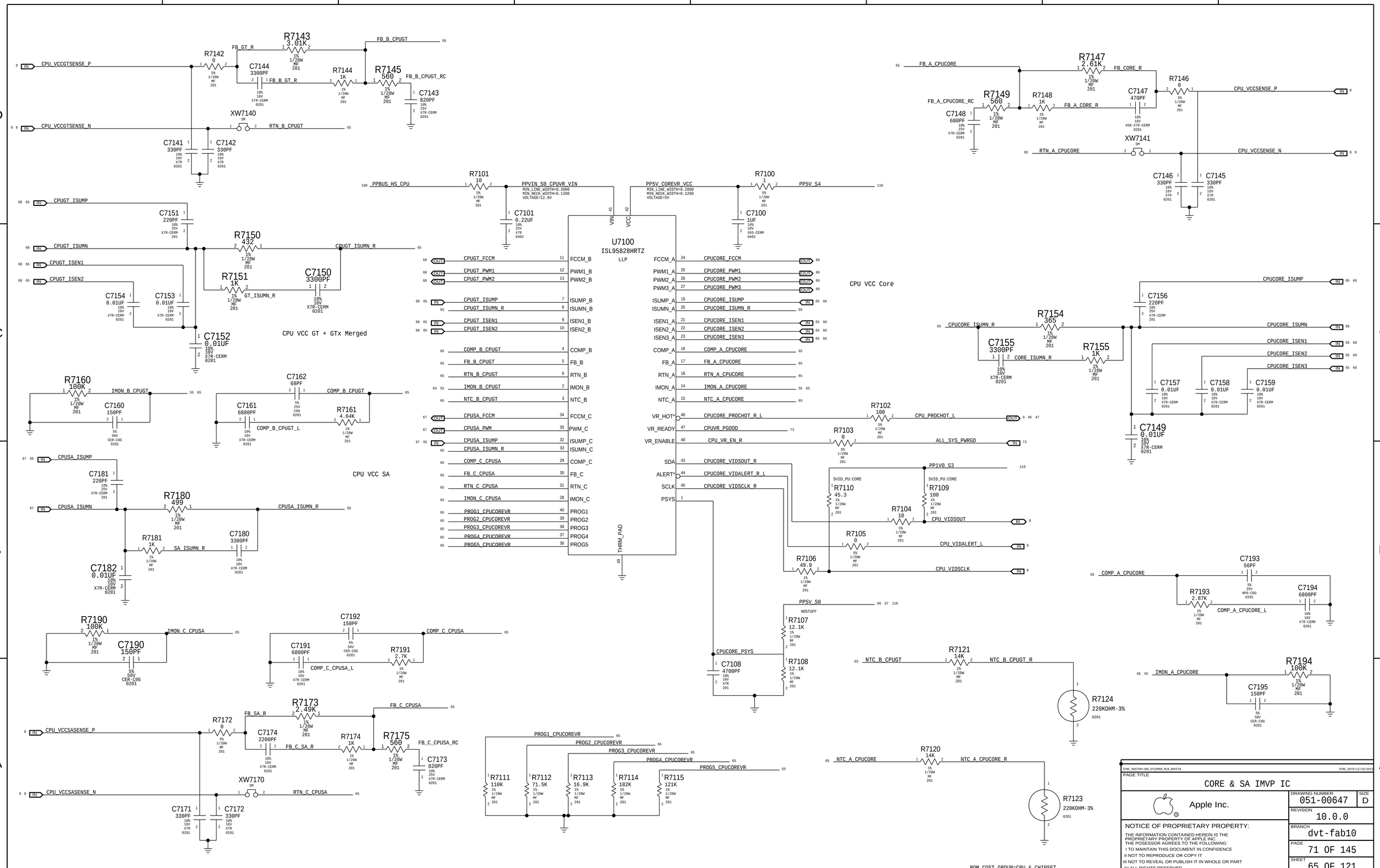
CPU VCC Core
CPU VCC GT + GTx Merged
CPU VCC SA
U7100
ISL95828HRTZ
LLP
R7143 3.01K
R7142 0
C7144 3300PF
R7144 1K
R7145 560
C7143 820PF
XW7140
C7141 330PF
C7142 330PF
R7147 2.61K
R7149 560
R7148 1K
C7147 470PF
R7146 0
C7148 680PF
XW7141
C7146 330PF
C7145 330PF
R7101 10
C7101 0.22UF
R7100 1
C7100 1UF
C7151 220PF
R7150 432
R7151 1K
C7150 3300PF
C7154 0.01UF
C7153 0.01UF
C7152 0.01UF
R7154 365
C7155 3300PF
R7155 1K
C7156 220PF
C7157 0.01UF
C7158 0.01UF
C7159 0.01UF
C7149 0.01UF
R7160 100K
C7160 150PF
C7162 68PF
C7161 6800PF
R7161 4.64K
C7181 220PF
R7180 499
R7181 1K
C7180 3300PF
C7182 0.01UF
R7102 100
R7103 0
R7110 45.3
R7109 100
R7104 10
R7105 0
R7106 49.9
R7107 12.1K
R7108 12.1K
C7108 4700PF
R7121 14K
R7124 220KOHM-3%
C7193 56PF
R7193 2.87K
C7194 6800PF
R7190 100K
C7190 150PF
C7192 150PF
C7191 6800PF
R7191 2.7K
R7194 100K
C7195 150PF
R7173 2.49K
R7172 0
C7174 2200PF
R7174 1K
R7175 560
C7173 820PF
XW7170
C7171 330PF
C7172 330PF
R7111 110K
R7112 71.5K
R7113 16.9K
R7114 182K
R7115 121K
R7120 14K
R7123 220KOHM-3%
BOM_COST_GROUP=CPU & CHIPSET
SYNC_MASTER=J80_DT32MAN_MLB_BAFFIN
SYNC_DATE=12/10/2012
PAGE TITLE
CORE & SA IMVP IC
Apple Inc.
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
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SHEET 65 OF 121
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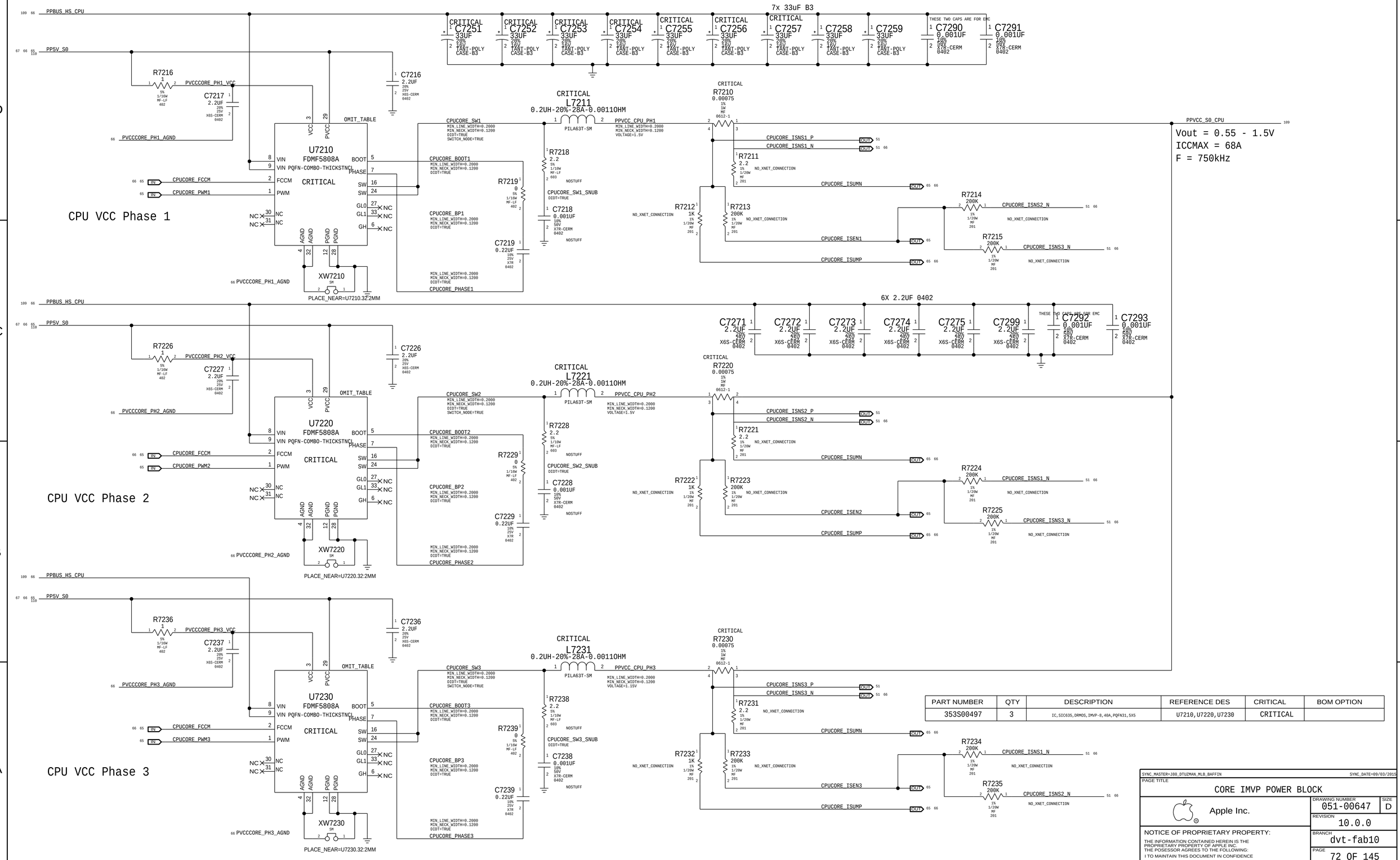

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00497	3	IC,SIC635,DRMOS,IMVP-8,40A,PQFN31,5X5	U7210,U7220,U7230	CRITICAL	

SYNC_MASTER=J89_DTUZMAN_MLB_BAFFIN SYNC_DATE=09/03/2015

PAGE TITLE
CORE IMVP POWER BLOCK

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
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SHEET 66 OF 121

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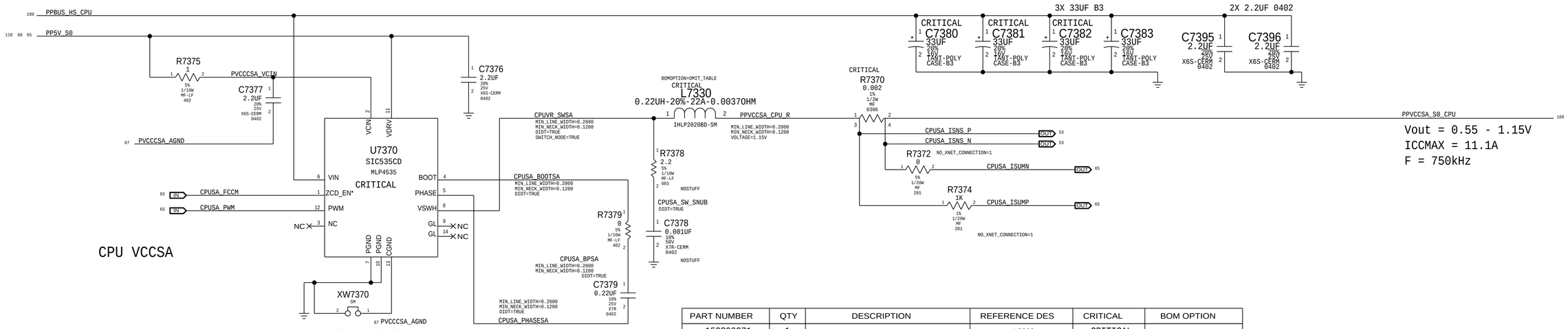

Vout = 0.55 - 1.15V
ICCMAX = 11.1A
F = 750kHz

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00371	1	IND,MLD,0.22UH,20%,22A,3.7MO,5.1x5.2x2.4	L7330	CRITICAL	

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J80_DTUZMAN_MLB_BAFFIN SYNC_DATE=11/18/2015

PAGE TITLE
SA IMVP IC

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 73 OF 145
SHEET 67 OF 121

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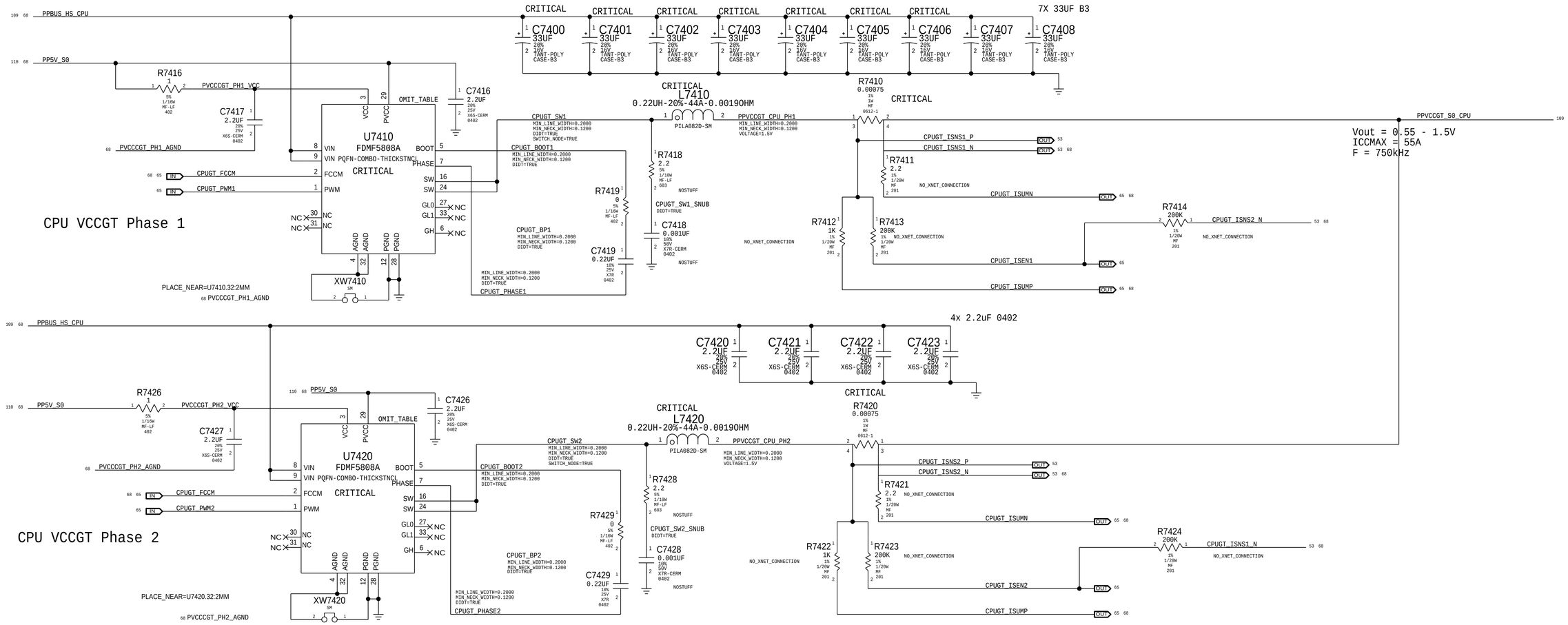

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00497	2	IC,SIC635,DRMOS,IMVP-8,40A,PQFN31,5X5	U7410,U7420	CRITICAL	

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J80_DTSUZMAR_MLB_BAFFIN SYNC_DATE=09/03/2013

PAGE TITLE
GT & GTX IMVP POWER BLOCK

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SHEET 68 OF 121

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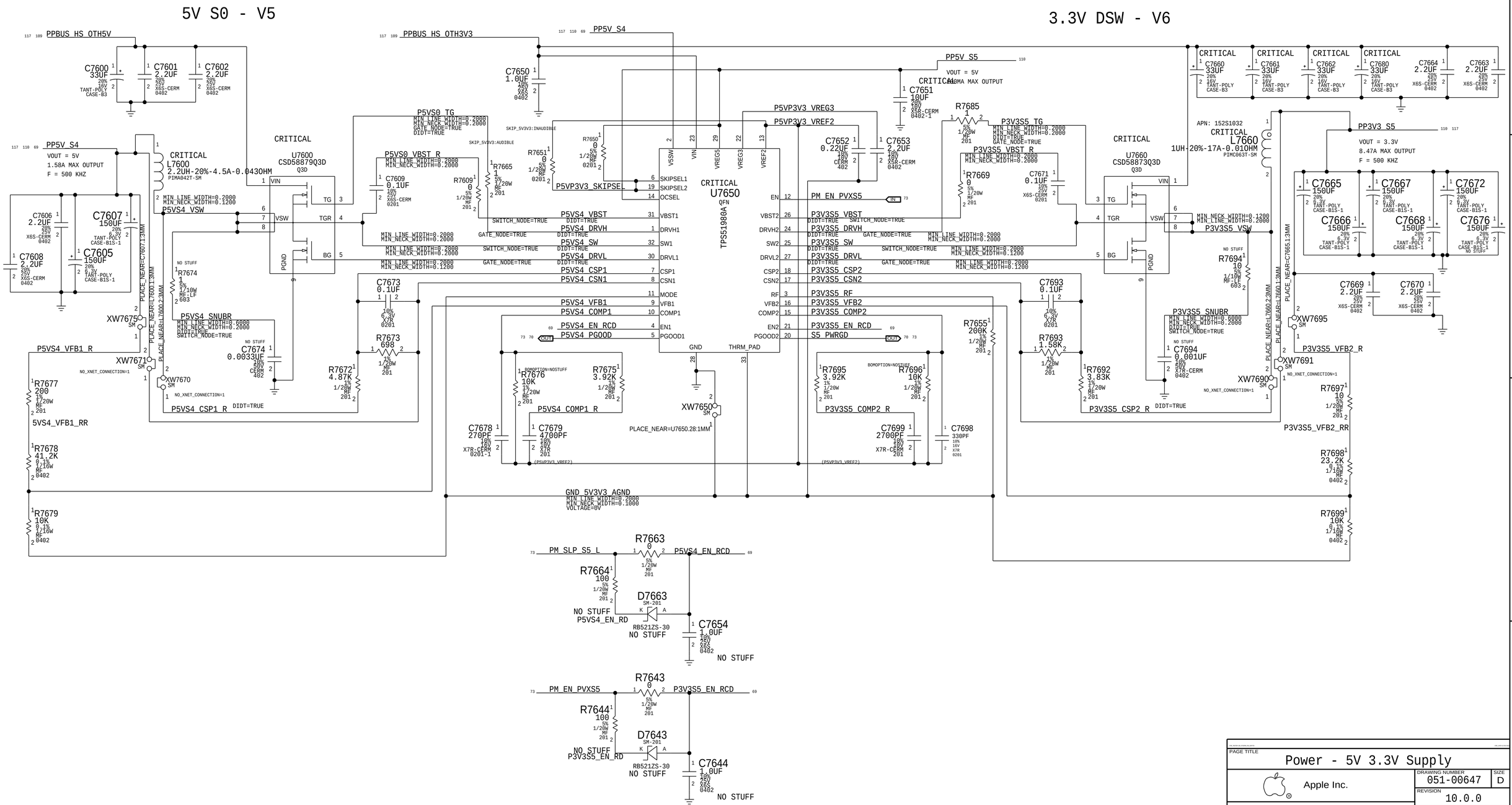

PAGE TITLE

Power - 5V 3.3V Supply

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

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SHEET 69 OF 121

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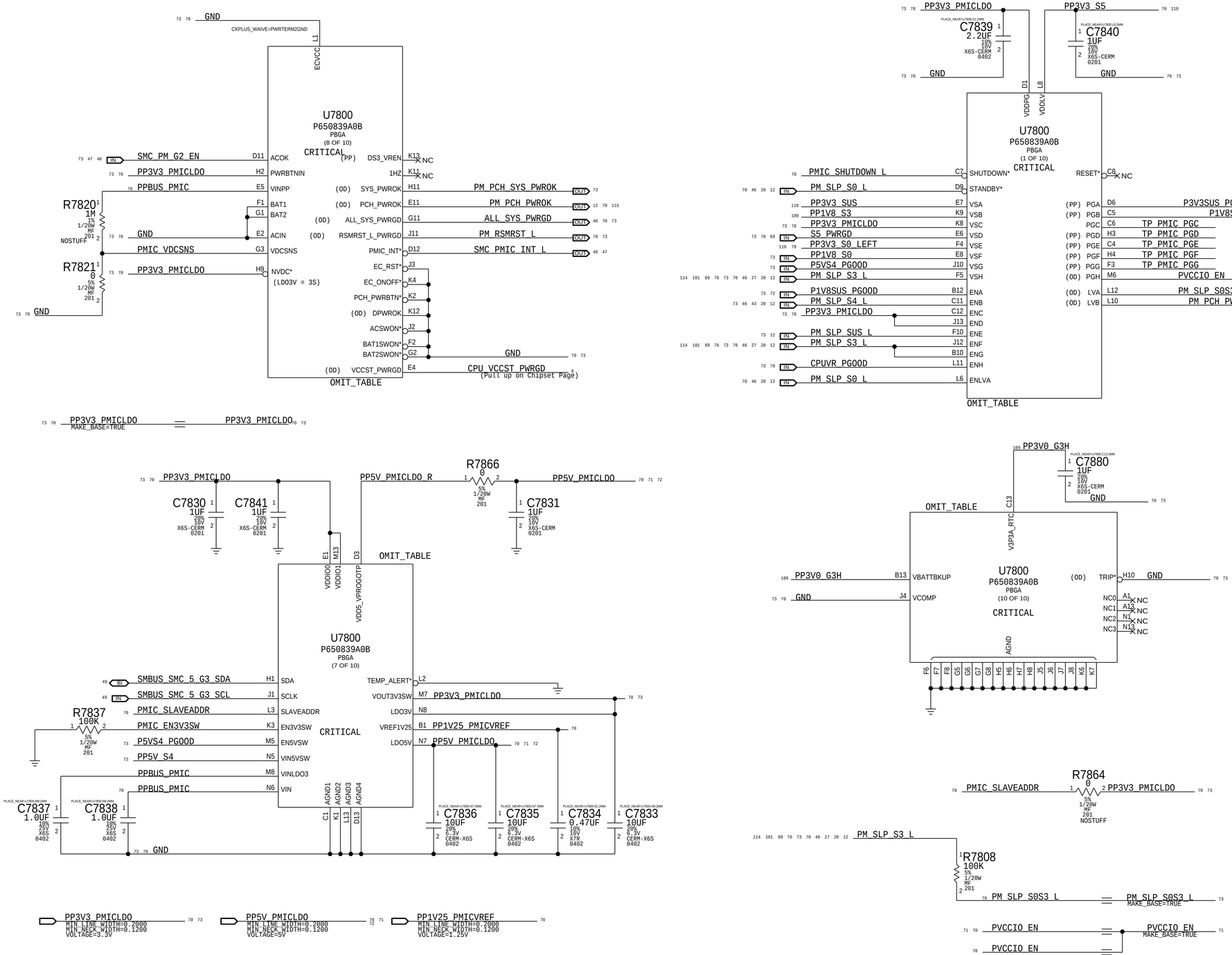
BANJO - PMIC Control



PAGE TITLE

PMIC-1 & Power Control

Apple Inc.

DRAWING NUMBER 051-00647 | SIZE D

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SHEET 70 OF 121

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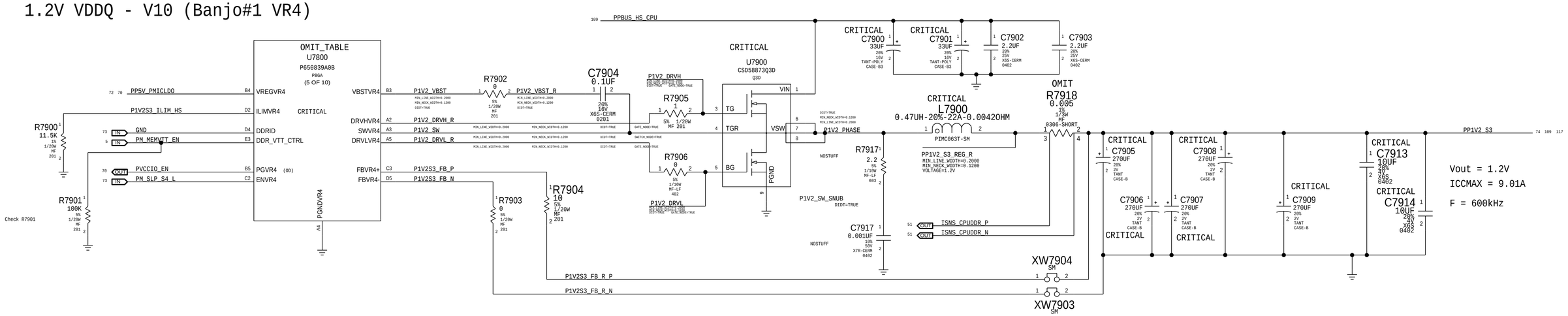
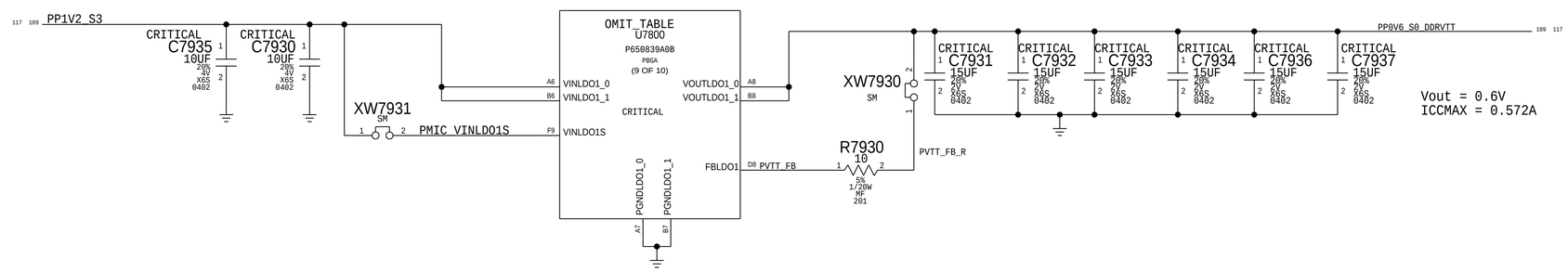
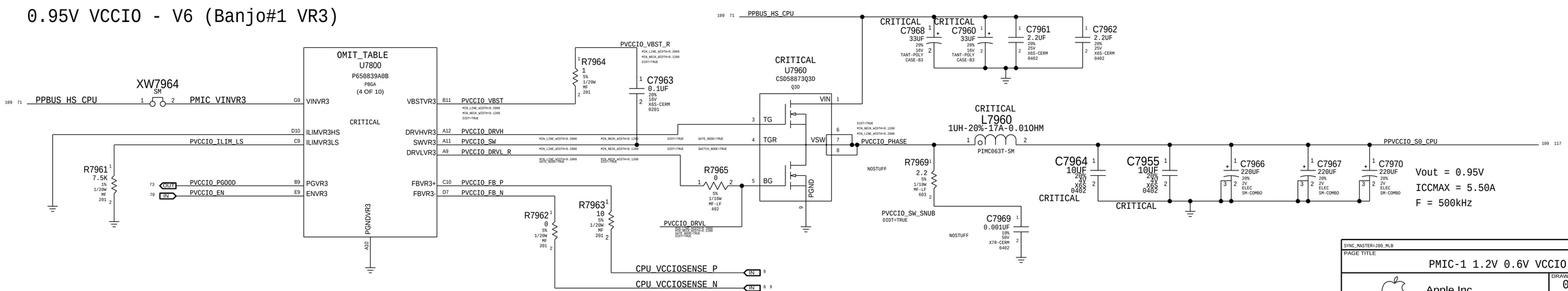
1.2V VDDQ - V10 (Banjo#1 VR4)



0.6V VTT - V13 (Banjo#1 LDO1)



0.95V VCCIO - V6 (Banjo#1 VR3)



BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE

PMIC-1 1.2V 0.6V VCCIO

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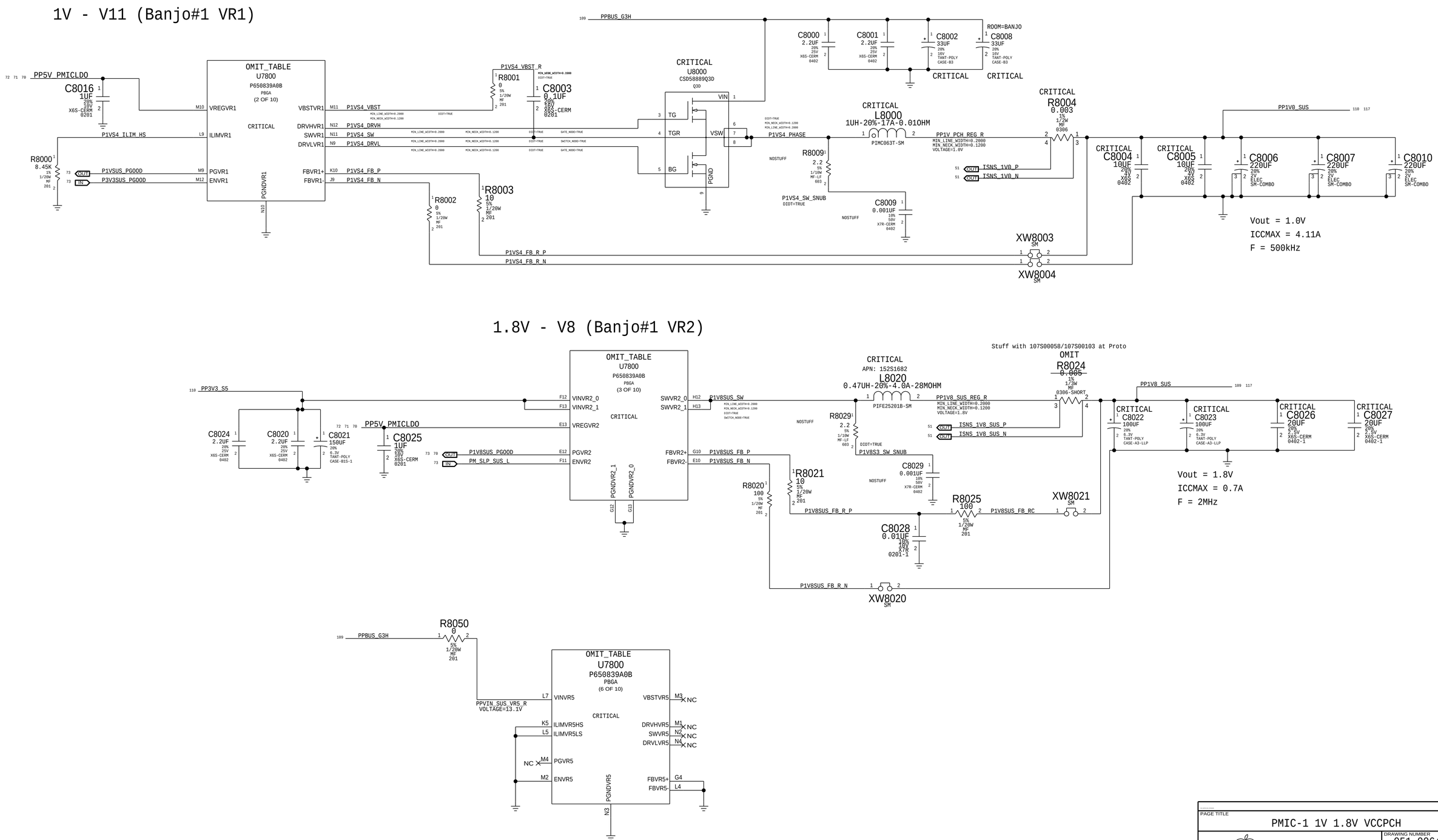
SHEET 71 OF 121



BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE	PMIC-1 1V 1.8V VCCPCH
Apple Inc.	DRAWING NUMBER 051-00647 SIZE D
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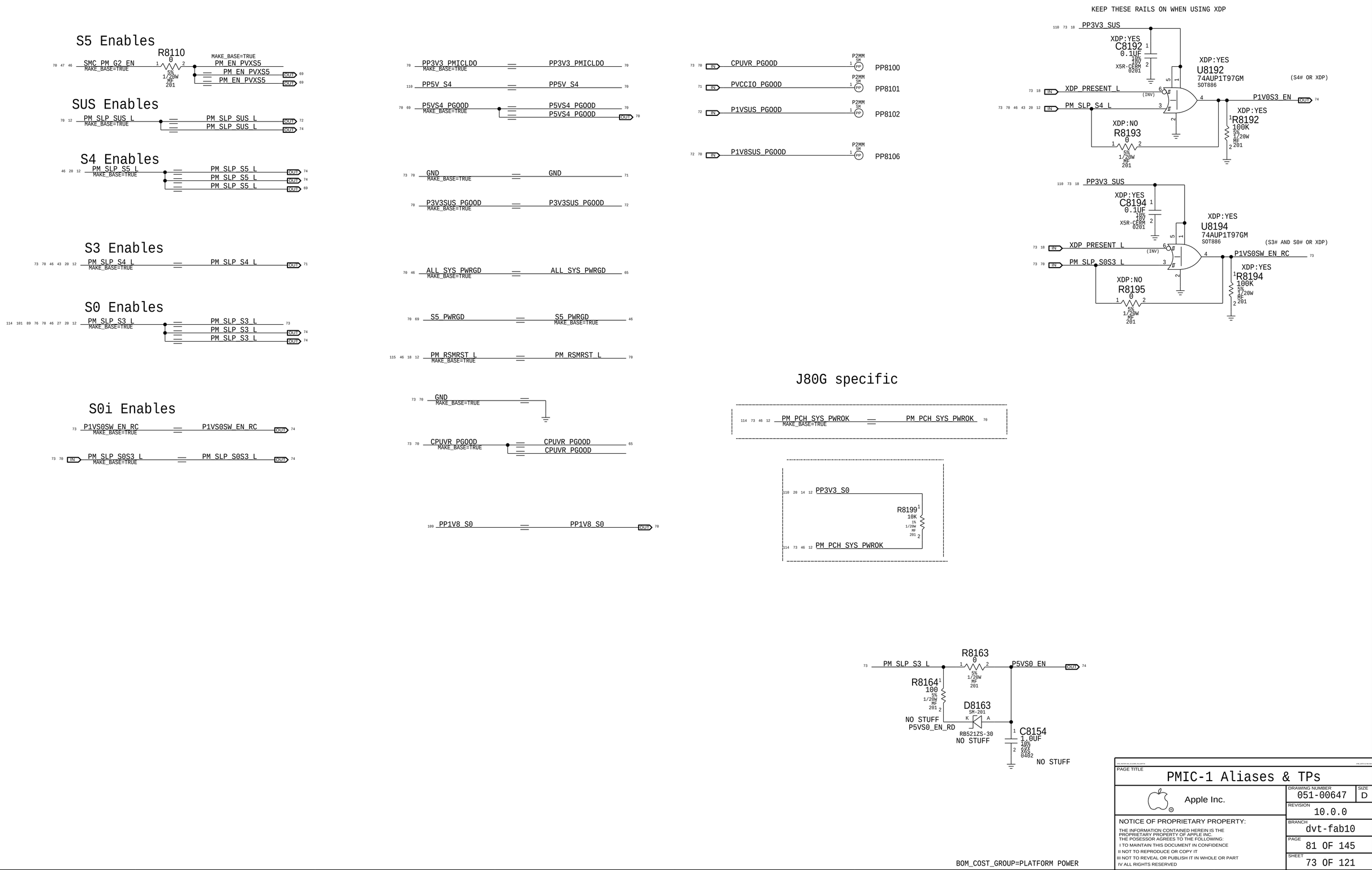
	PAGE 80 OF 145
	SHEET 72 OF 121



PAGE TITLE

PMIC-1 Aliases & TPs

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

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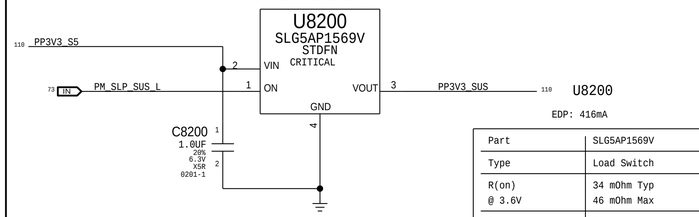
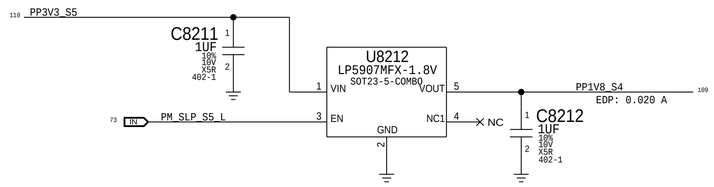
3.3V SUS Switch

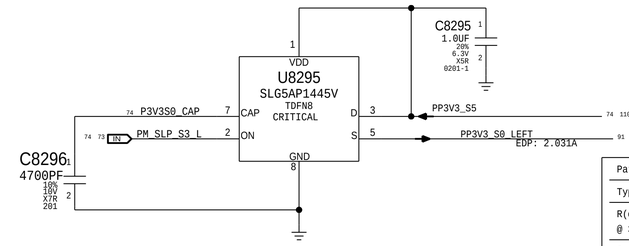


Part	SLG5AP1569V
Type	Load Switch
R(on) @ 3.6V	34 mOhm Typ 46 mOhm Max
Current	1A Max

1.8V S4 LDO

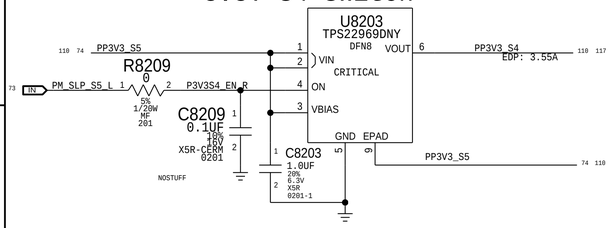


3.3V S0 Switch LEFT



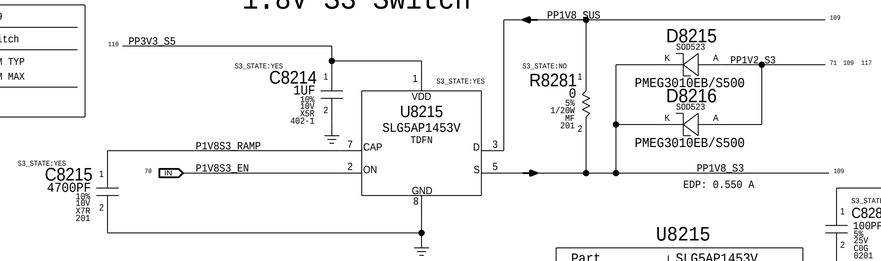
Part	SLG5AP1445V
Type	Load Switch
R(on) @ 3.6V	7.8 MOHM TYP 8.5 MOHM MAX
Current	4A MAX

3.3V S4 Switch



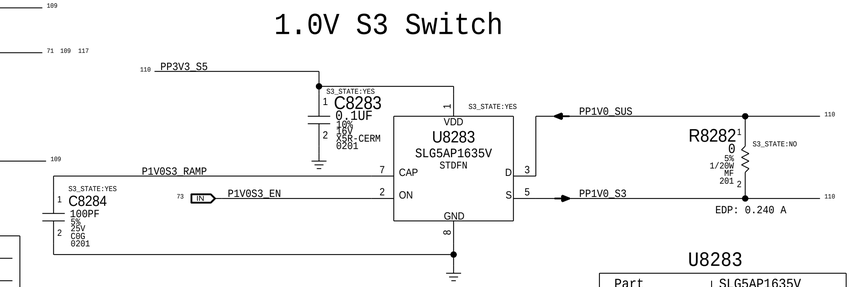
Part	TPS22969
Type	Load Switch
R(on) @ 3.6V	4.4 MOHM TYP 6.6 MOHM MAX
Current	6A MAX

1.8V S3 Switch



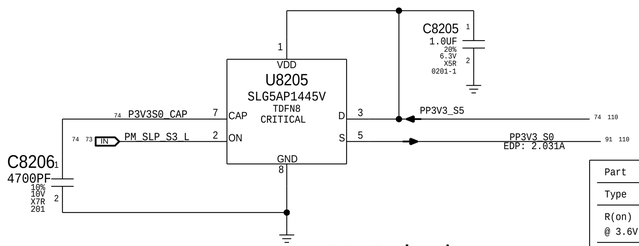
Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

1.0V S3 Switch



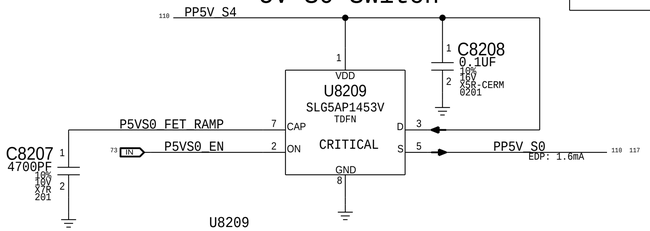
Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 mOhm Typ 28 mOhm Max
Current	2.5A Max
Ton Total	39us max @ 1V

3.3V S0 Switch



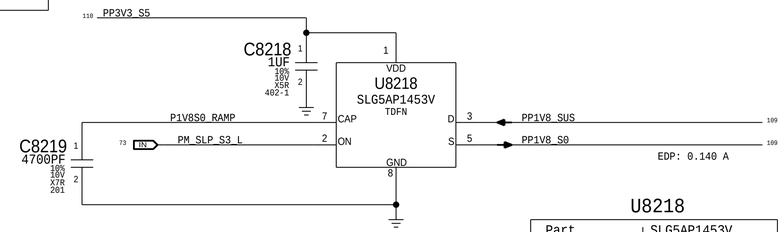
Part	SLG5AP1445V
Type	Load Switch
R(on) @ 3.6V	7.8 MOHM TYP 8.5 MOHM MAX
Current	4A MAX

5V S0 Switch



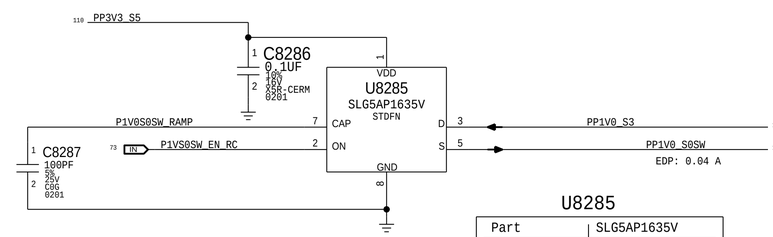
Part	SLG5AP1453V
Type	Load Switch
R(on)	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A

1.8V S0 Switch



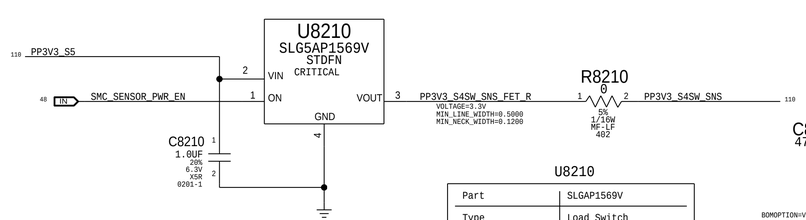
Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

1.0V S0 SW Switch



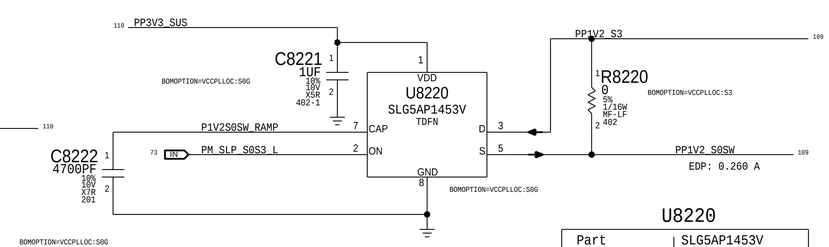
Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 mOhm Typ 28 mOhm Max
Current	2.5A Max
Ton Total	39us max @ 1V

3.3V Sensor Switch



Part	SLGAP1569V
Type	Load Switch
R(on) @ 3.6V	34 mOhm Typ 46 mOhm Max
Current	1A Max

1.2V S0 SW Switch



Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE

Power FETs

Apple Inc.

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DRAWING NUMBER	051-00647
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REVISION	10.0.0
BRANCH	dvt-fab10
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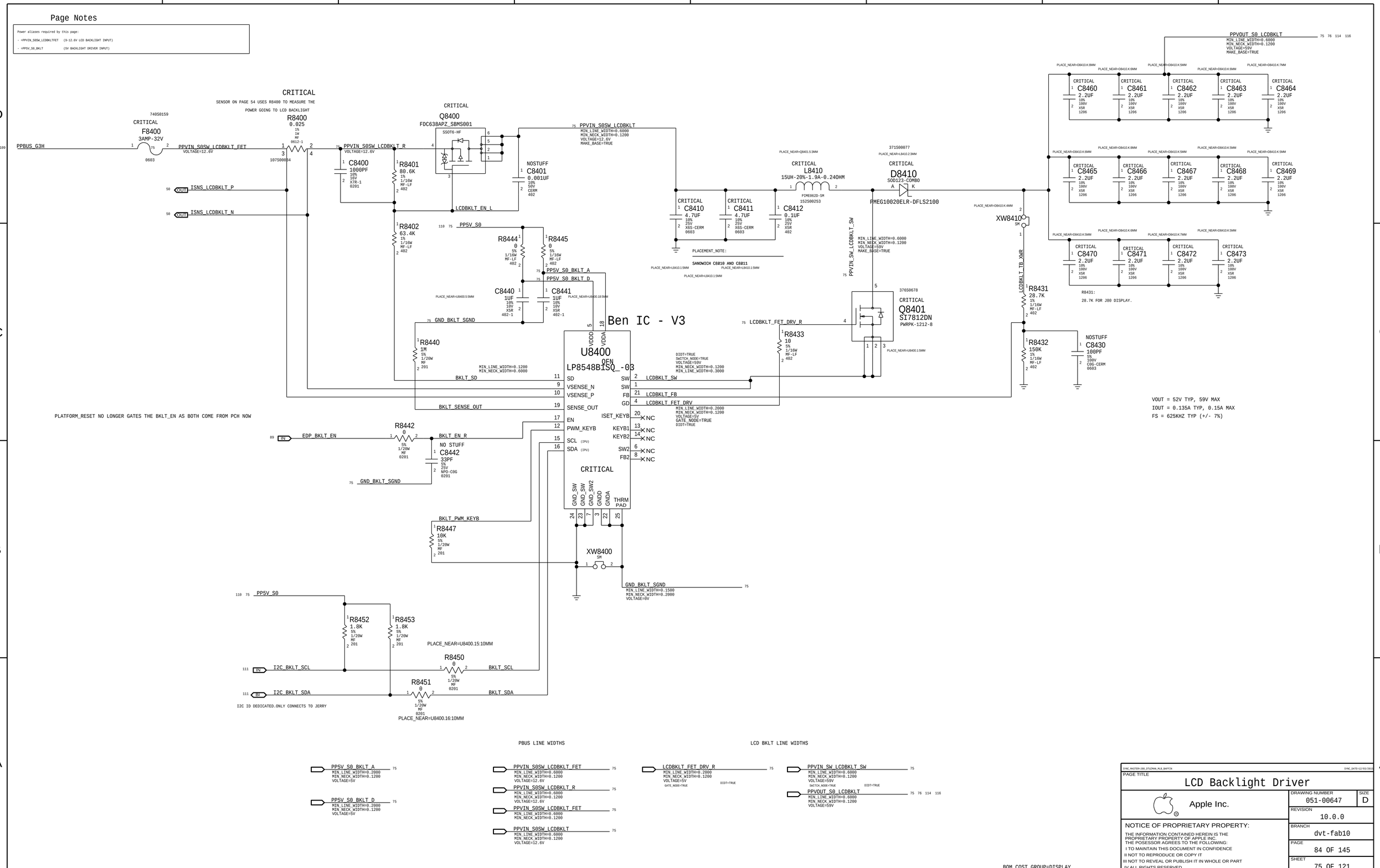
Page Notes
Power aliases required by this page:
- =PPVIN_S0SW_LCDBKLTFET (9-12.6V LCD BACKLIGHT INPUT)
- =PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)
CRITICAL
SENSOR ON PAGE 54 USES R8400 TO MEASURE THE
POWER GOING TO LCD BACKLIGHT
PPBUS_G3H
F8400
3AMP-32V
PPVIN_S0SW_LCDBKLT_FET
VOLTAGE=12.6V
R8400
0.025
PPVIN_S0SW_LCDBKLT_R
Q8400
FDC638APZ_SBMS001
SSOT6-HF
C8400
1000PF
R8401
80.6K
NOSTUFF
C8401
0.001UF
PPVIN_S0SW_LCDBKLT
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=12.6V
MAKE_BASE=TRUE
ISNS_LCDBKLT_P
ISNS_LCDBKLT_N
LCDBKLT_EN_L
R8402
63.4K
PP5V_S0
R8444
R8445
PP5V_S0_BKLT_A
PP5V_S0_BKLT_D
C8440
1UF
C8441
1UF
GND_BKLT_SGND
R8440
1M
Ben IC - V3
U8400
LP8548BISQ_-03
VDDD
VDDA
SD
VSENSE_N
VSENSE_P
SENSE_OUT
EN
PWM_KEYB
SCL
SDA
SW
FB
GD
ISET_KEYB
KEYB1
KEYB2
SW2
FB2
GND_SW
GND_SW2
GNDD
GNDA
THRM PAD
BKLT_SD
BKLT_SENSE_OUT
LCDBKLT_SW
LCDBKLT_FB
LCDBKLT_FET_DRV
DIDT=TRUE
SWITCH_NODE=TRUE
VOLTAGE=50V
MIN_NECK_WIDTH=0.1200
MIN_LINE_WIDTH=0.3000
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=5V
GATE_NODE=TRUE
DIDT=TRUE
PLATFORM_RESET NO LONGER GATES THE BKLT_EN AS BOTH COME FROM PCH NOW
R8442
EDP_BKLT_EN
BKLT_EN_R
NO STUFF
C8442
33PF
GND_BKLT_SGND
BKLT_PWM_KEYB
R8447
10K
XW8400
GND_BKLT_SGND
MIN_LINE_WIDTH=0.1500
MIN_NECK_WIDTH=0.2000
VOLTAGE=0V
R8452
1.8K
R8453
1.8K
PLACE_NEAR=U8400.15:10MM
R8450
I2C_BKLT_SCL
BKLT_SCL
R8451
I2C_BKLT_SDA
BKLT_SDA
I2C ID DEDICATED.ONLY CONNECTS TO JERRY
PLACE_NEAR=U8400.16:10MM
L8410
15UH-20%-1.9A-0.24OHM
PIME062D-SM
152S00253
C8410
4.7UF
C8411
4.7UF
C8412
0.1UF
PLACEMENT_NOTE:
SANDWICH C8410 AND C8411
D8410
SDD123-COMBO
PMEG10020ELR-DFLS2100
PPVIN_SW_LCDBKLT_SW
Q8401
SI7812DN
PWRPK-1212-8
R8433
10
XW8410
LCDBKLT_TB_XWR
R8431
28.7K
R8431:
28.7K FOR J80 DISPLAY.
R8432
150K
NOSTUFF
C8430
100PF
PPVOUT_S0_LCDBKLT
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=50V
MAKE_BASE=TRUE
C8460
C8461
C8462
C8463
C8464
C8465
C8466
C8467
C8468
C8469
C8470
C8471
C8472
C8473
2.2UF
VOUT = 52V TYP, 59V MAX
IOUT = 0.135A TYP, 0.15A MAX
FS = 625KHZ TYP (+/- 7%)
PBUS LINE WIDTHS
PP5V_S0_BKLT_A
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=5V
PP5V_S0_BKLT_D
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=5V
PPVIN_S0SW_LCDBKLT_FET
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=12.6V
PPVIN_S0SW_LCDBKLT_R
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=12.6V
PPVIN_S0SW_LCDBKLT_FET
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
PPVIN_S0SW_LCDBKLT
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=12.6V
LCD BKLT LINE WIDTHS
LCDBKLT_FET_DRV_R
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=5V
GATE_NODE=TRUE
DIDT=TRUE
PPVIN_SW_LCDBKLT_SW
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=50V
SWITCH_NODE=TRUE
DIDT=TRUE
PPVOUT_S0_LCDBKLT
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=50V
BOM_COST_GROUP=DISPLAY
PAGE TITLE
LCD Backlight Driver
Apple Inc.
DRAWING NUMBER
051-00647
SIZE
D
REVISION
10.0.0
BRANCH
dvt-fab10
PAGE
84 OF 145
SHEET
75 OF 121
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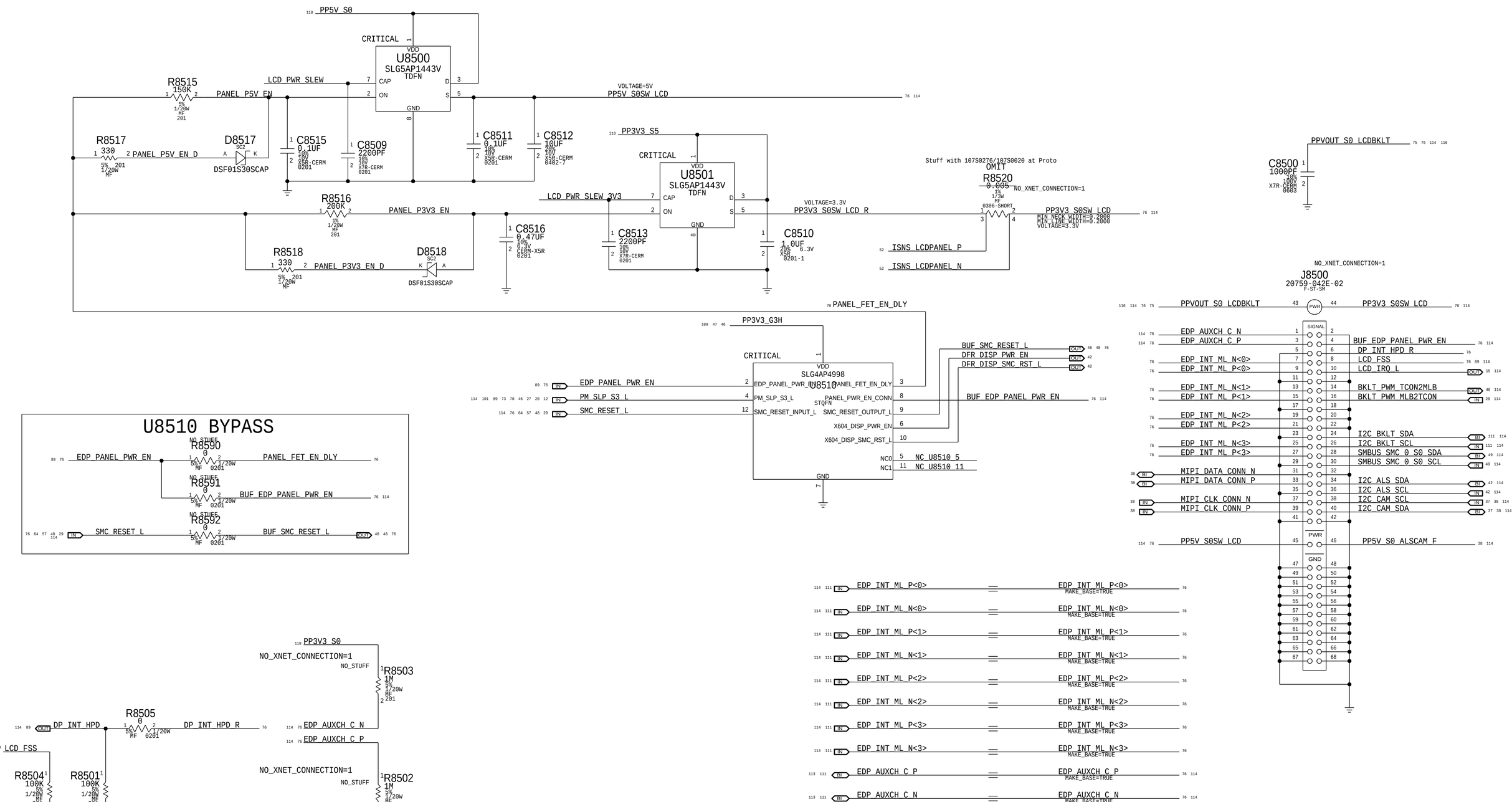
LCD PANEL INTERFACE (eDP) + Camera (MIPI)



LCD Panel HPD, FSS & AUX strapping

PAGE TITLE
eDP Display Connector

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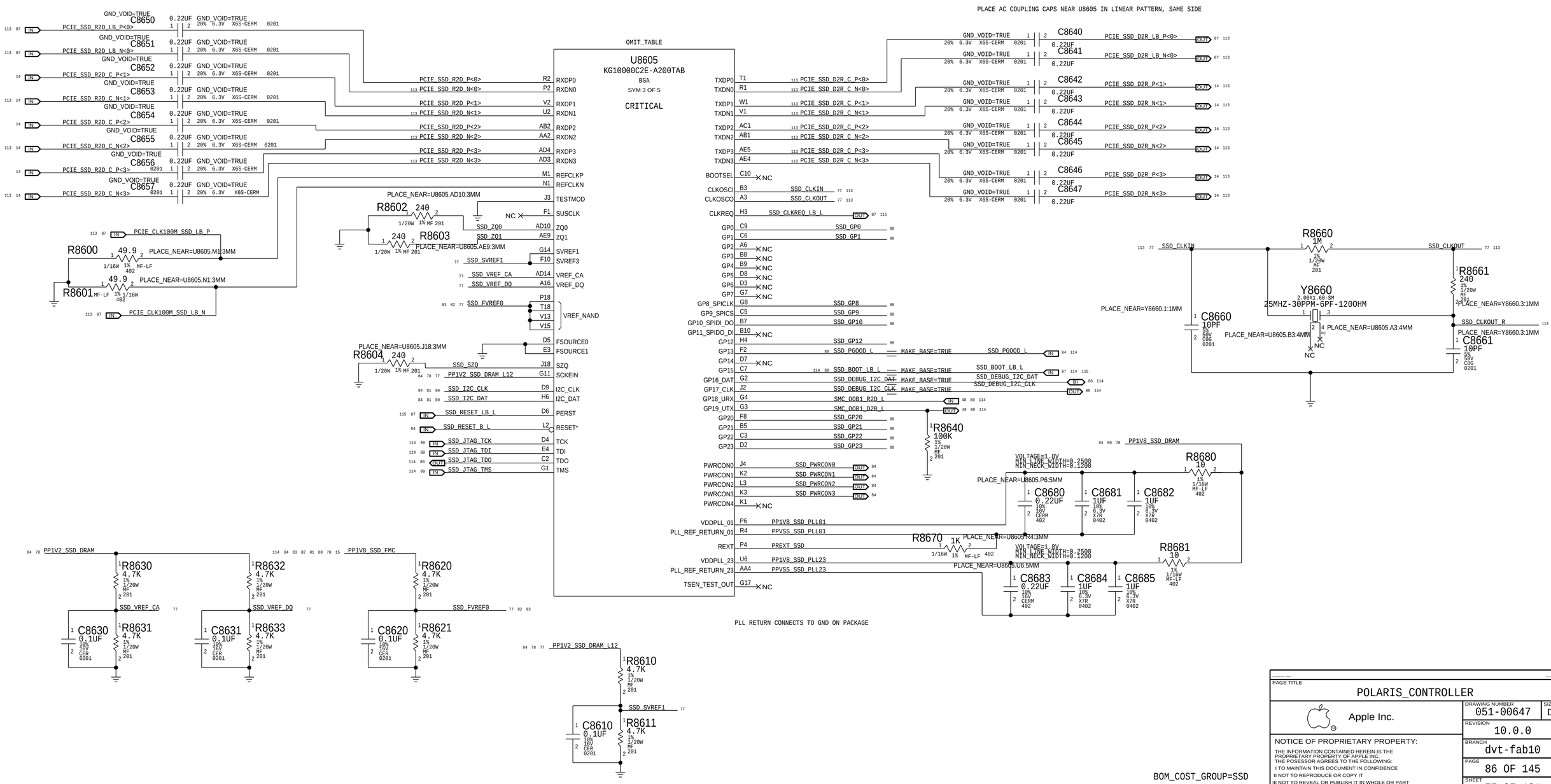
PLACE AC COUPLING CAPS NEAR U8605 IN LINEAR PATTERN, SAME SIDE
OMIT_TABLE
U8605
KG10000C2E-A200TAB
BGA
SYM 3 OF 5
CRITICAL
PLL RETURN CONNECTS TO GND ON PACKAGE
BOM_COST_GROUP=SSD
PAGE TITLE
POLARIS_CONTROLLER
Apple Inc.
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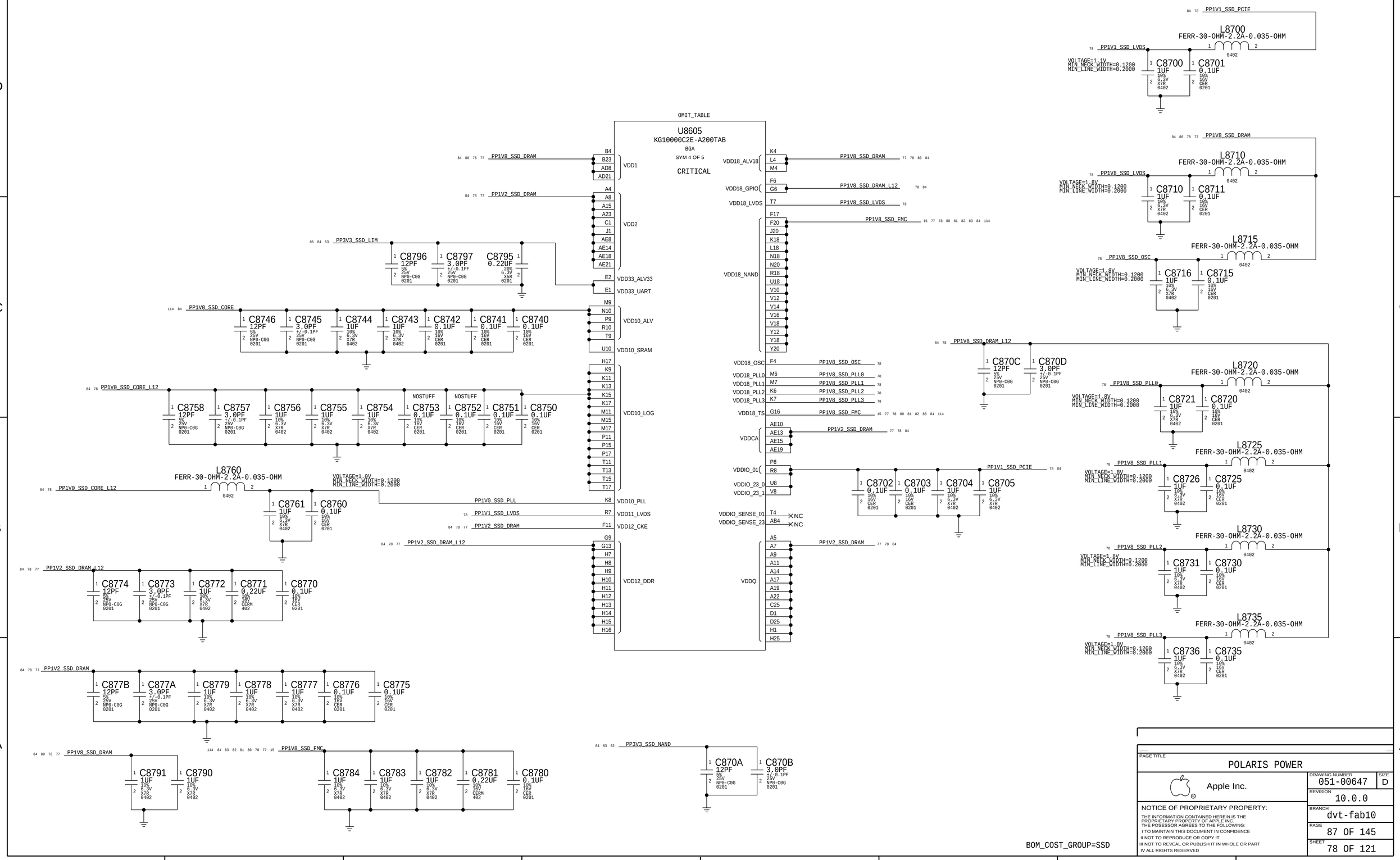

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POLARIS POWER

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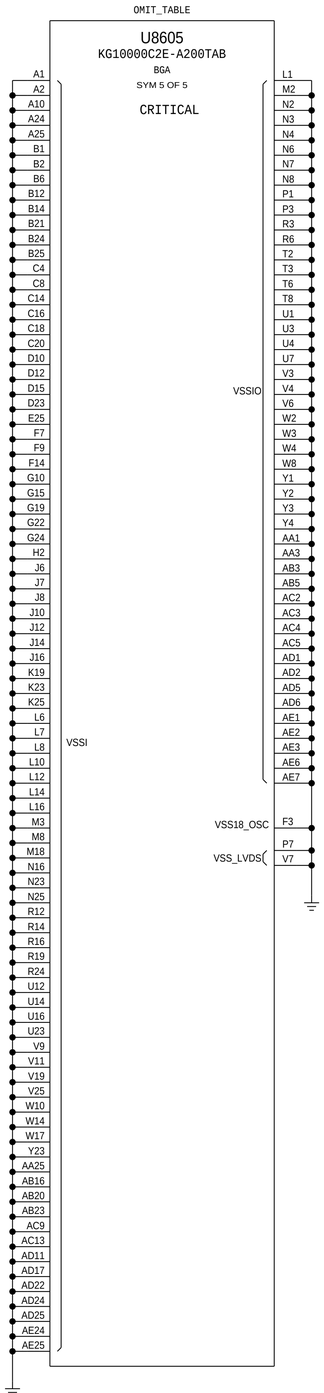

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PAGE TITLE

PAGE_TITLE=POLARIS GND

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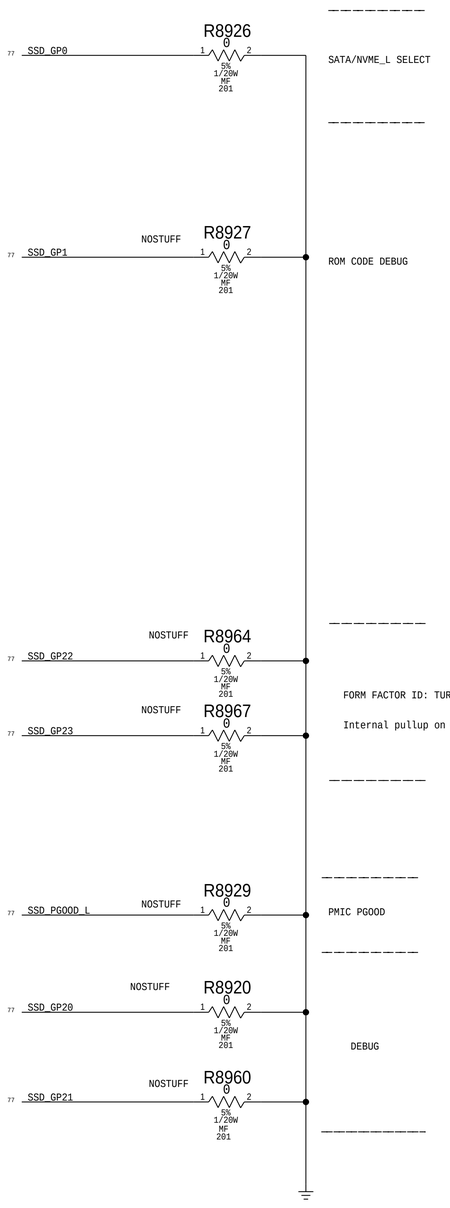
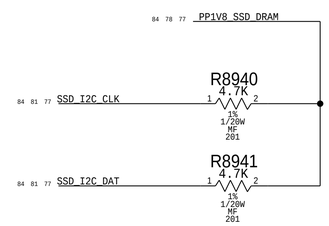
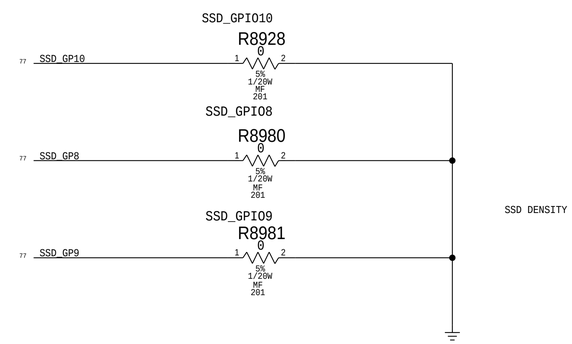






SSD RELATED BOM Groups

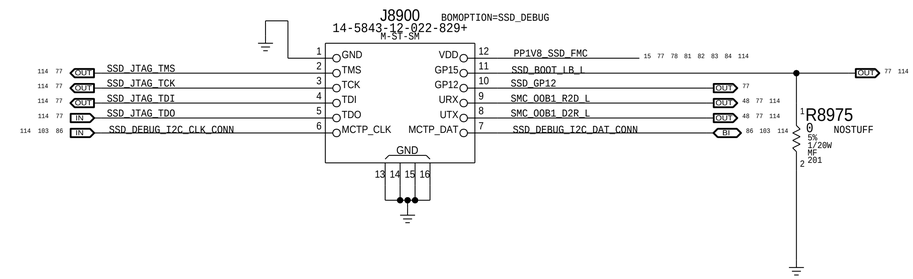
BOM GROUP	BOM OPTIONS
SSD_CONFIG:256GB	SSD_GPIO9,NAND_TYPE:256GB,SSD_CTRL_TYPE:4GBIT
SSD_CONFIG:512GB	SSD_GPIO8,NAND_TYPE:512GB,SSD_CTRL_TYPE:4GBIT
SSD_CONFIG:1TB	NAND_TYPE:1TB,SSD_CTRL_TYPE:8GBIT
SSD_CONFIG:2TB	SSD_GPIO10,NAND_TYPE:2TB,SSD_CTRL_TYPE:8GBIT

NAND Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00149	4	NAND,1Z,64GBM,TOGG DDR2,64G,SS,BGA 168	U9100,U9110,U9200,U9210	CRITICAL	NAND_TYPE:256GB
335S00204	4	NAND,V3,128GBM,TOGG DDR2,256G,SSBGA 168	U9100,U9110,U9200,U9210	CRITICAL	NAND_TYPE:512GB
335S00205	4	NAND,V3,256GBM,TOGG DDR2,256G,SS,BGA 168	U9100,U9110,U9200,U9210	CRITICAL	NAND_TYPE:1TB
335S00219	4	NAND,V3,512GBM,TOGG DDR2,256G,SS,BGA 168	U9100,U9110,U9200,U9210	CRITICAL	NAND_TYPE:2TB

SSD Controller Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
339S00154	1	POP,POLARIS+4GBIT,SSD CTRL,A2,BGA516	U8605	CRITICAL	SSD_CTRL_TYPE:4GBIT
339S00155	1	POP,POLARIS+8GBIT,SSD CTRL,A2,BGA516	U8605	CRITICAL	SSD_CTRL_TYPE:8GBIT



SSD CONFIGURATIONS

CAPACITY	NAND APN	CONTROLLER APN	R8980/GPIO8	R8981/GPIO9	R8928/GPIO10
128 GB	-	-	STUFF-0	STUFF-0	STUFF-0
256 GB	335S00149	339S00154 (A2 4GB DRAM)	NOSTUFF-1	STUFF-0	NOSTUFF-1
512 GB	335S00204	339S00154 (A2 4GB DRAM)	STUFF-0	NOSTUFF-1	NOSTUFF-1
1 TB	335S00205	339S00155 (A2 8GB DRAM)	NOSTUFF-1	NOSTUFF-1	NOSTUFF-1
2 TB	335S00219	339S00155 (A2 8GB DRAM)	NOSTUFF-1	NOSTUFF-1	STUFF-0

BOM_COST_GROUP=SSD

PAGE TITLE
Connector

Apple Inc.

DRAWING NUMBER 051-00647
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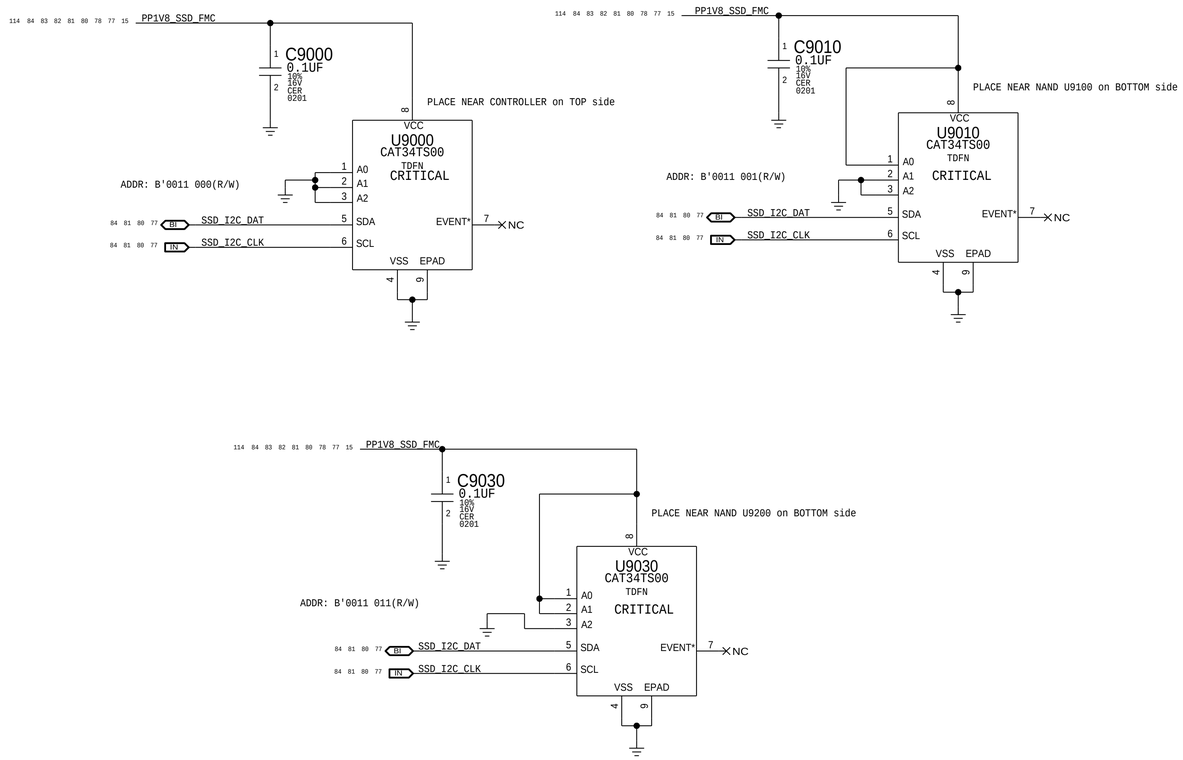

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PAGE TITLE	PAGE_TITLE=TEMP SENSORS
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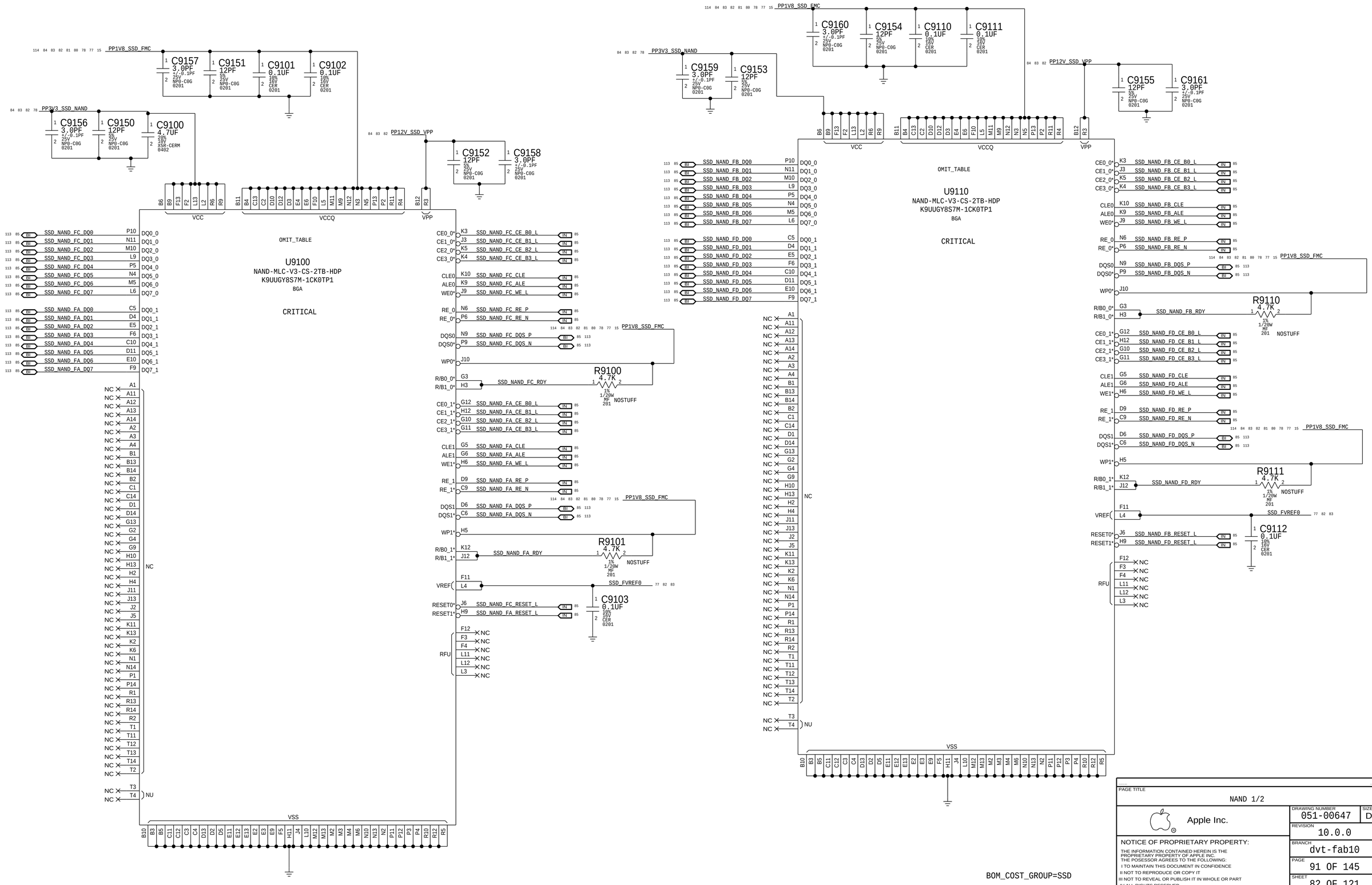

PAGE TITLE
NAND 1/2

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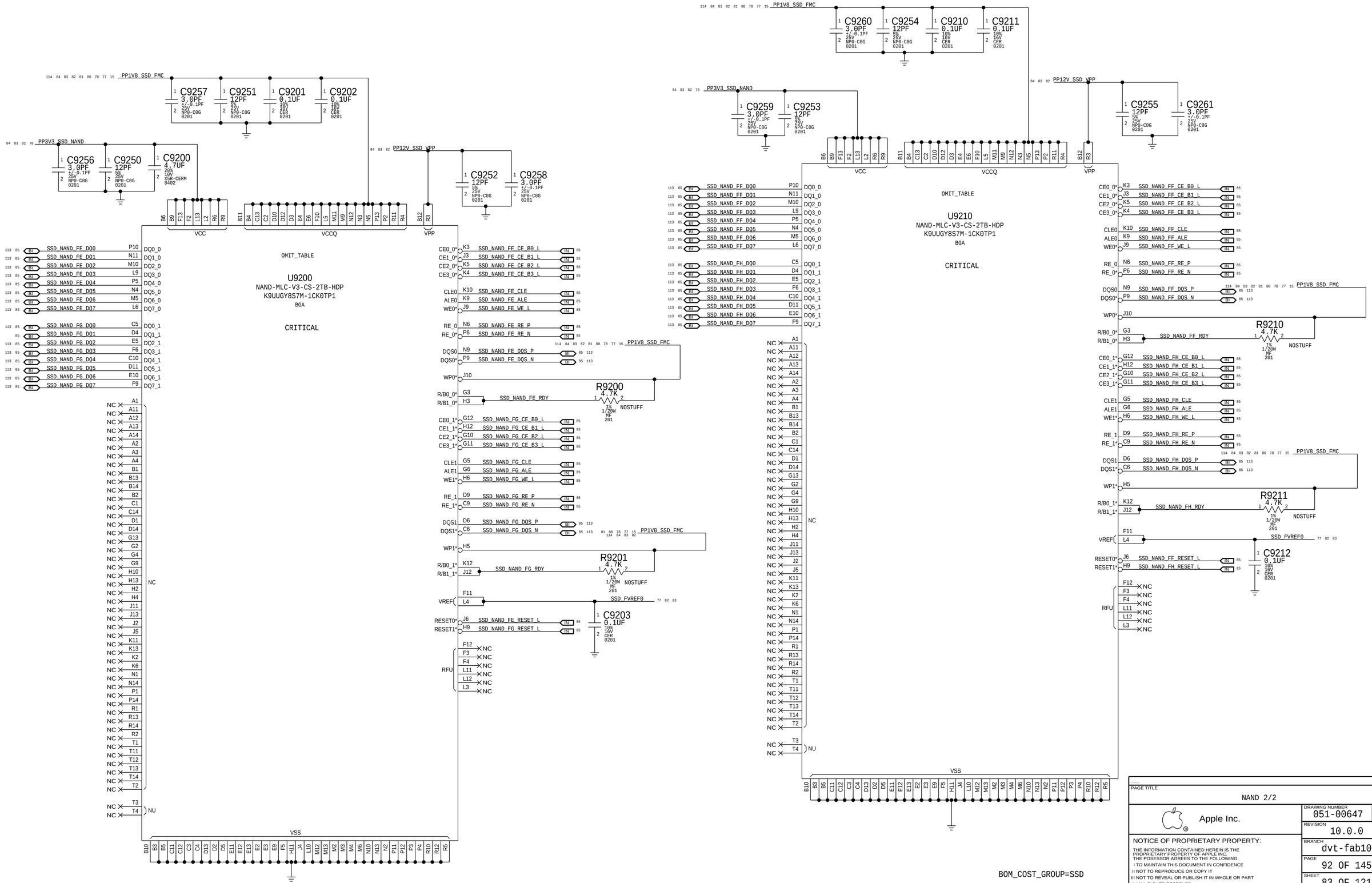
PP1V8_SSD_FMC
C9257 3.0PF ±/-0.1PF 25V NP0-C0G 0201
C9251 12PF 5% 25V NP0-C0G 0201
C9201 0.1UF 10% 16V CER 0201
C9202 0.1UF 10% 16V CER 0201
PP3V3_SSD_NAND
C9256 3.0PF ±/-0.1PF 25V NP0-C0G 0201
C9250 12PF 5% 25V NP0-C0G 0201
C9200 4.7UF 20% 10V X5R-CERM 0402
PP12V_SSD_VPP
C9252 12PF 5% 25V NP0-C0G 0201
C9258 3.0PF ±/-0.1PF 25V NP0-C0G 0201
VCC
VCCQ
VPP
OMIT_TABLE
U9200
NAND-MLC-V3-CS-2TB-HDP
K9UUGY8S7M-1CK0TP1
BGA
CRITICAL
SSD_NAND_FE_DQ0
SSD_NAND_FE_DQ1
SSD_NAND_FE_DQ2
SSD_NAND_FE_DQ3
SSD_NAND_FE_DQ4
SSD_NAND_FE_DQ5
SSD_NAND_FE_DQ6
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SSD_NAND_FG_CE_B0_L
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SSD_NAND_FG_RESET_L
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NC
NU
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C9253 12PF 5% 25V NP0-C0G 0201
PP12V_SSD_VPP
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OMIT_TABLE
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BGA
CRITICAL
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SSD_NAND_FF_RE_P
SSD_NAND_FF_RE_N
SSD_NAND_FF_DQS_P
SSD_NAND_FF_DQS_N
SSD_NAND_FF_RDY
R9210 4.7K 1% 1/20W MF 201 NOSTUFF
SSD_NAND_FH_CE_B0_L
SSD_NAND_FH_CE_B1_L
SSD_NAND_FH_CE_B2_L
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SSD_NAND_FH_RE_P
SSD_NAND_FH_RE_N
SSD_NAND_FH_DQS_P
SSD_NAND_FH_DQS_N
SSD_NAND_FH_RDY
R9211 4.7K 1% 1/20W MF 201 NOSTUFF
SSD_FVREF0
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SSD_NAND_FH_RESET_L
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NC
NU
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NAND 2/2
Apple Inc.
DRAWING NUMBER 051-00647
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REVISION 10.0.0
BRANCH dvt-fab10
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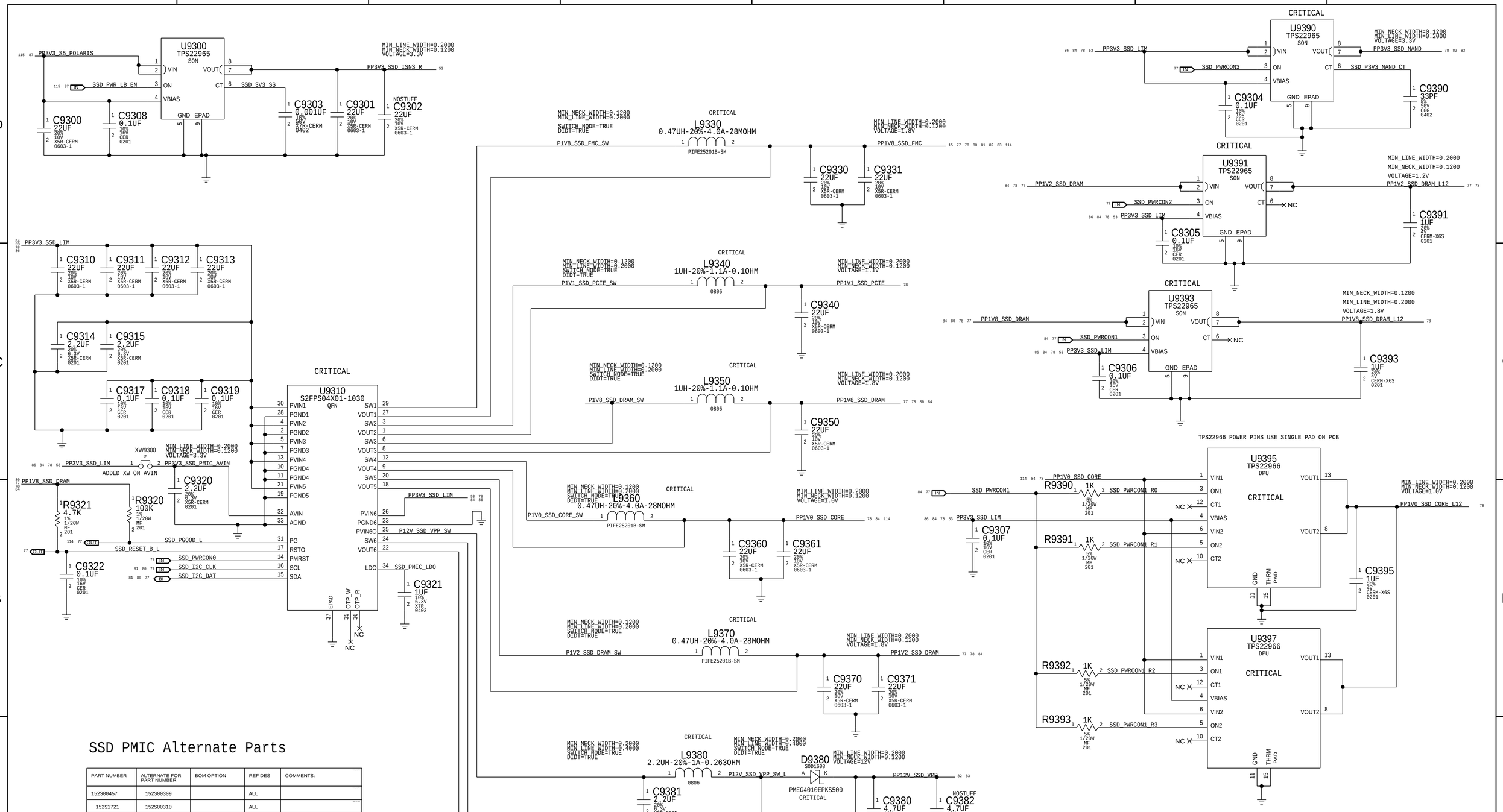

SSD PMIC Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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152S1721	152S00310		ALL	

PAGE TITLE

PAGE_TITLE=POLARIS PMIC

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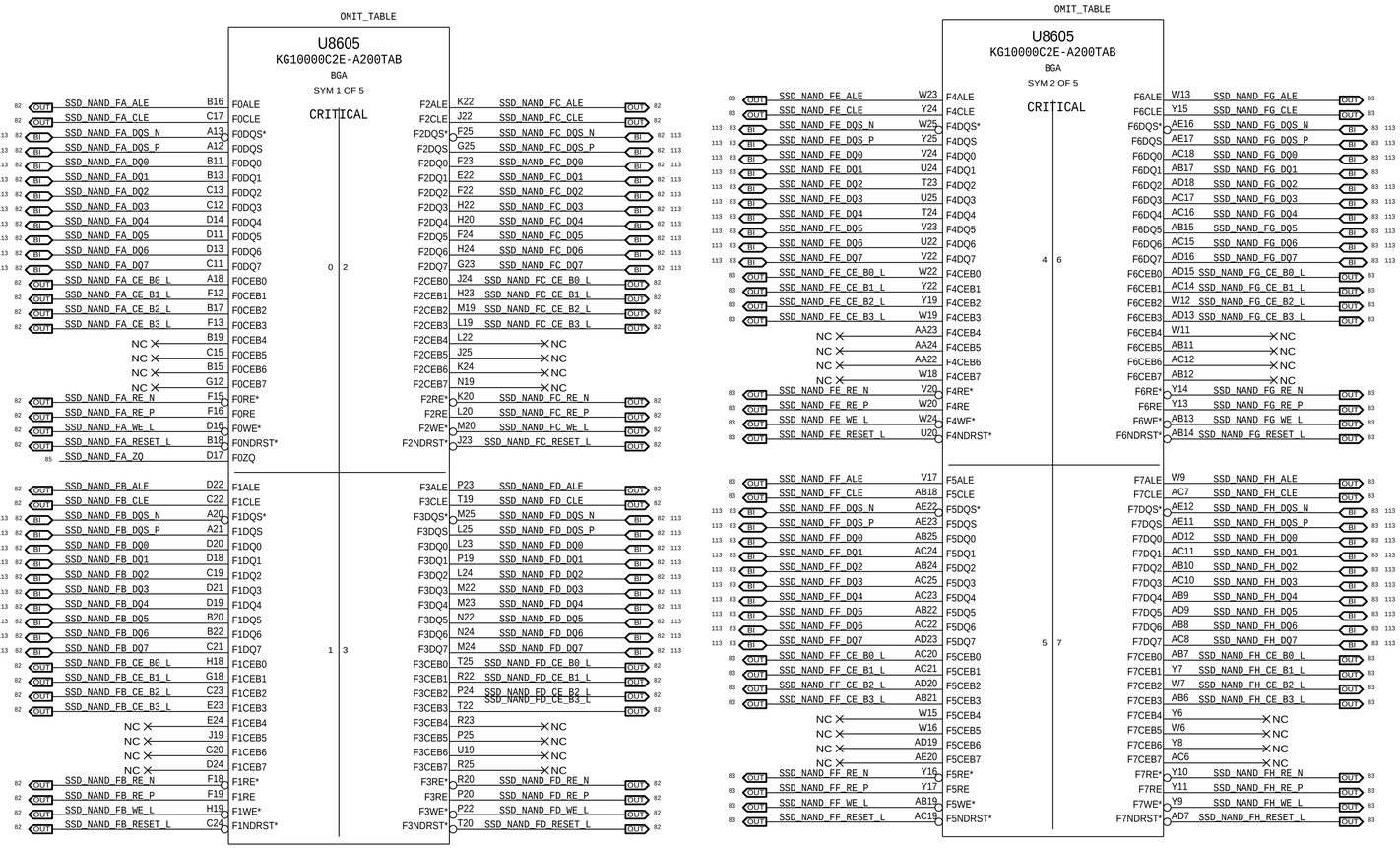

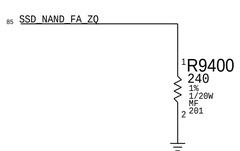

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PAGE TITLE
SSD NAND VR

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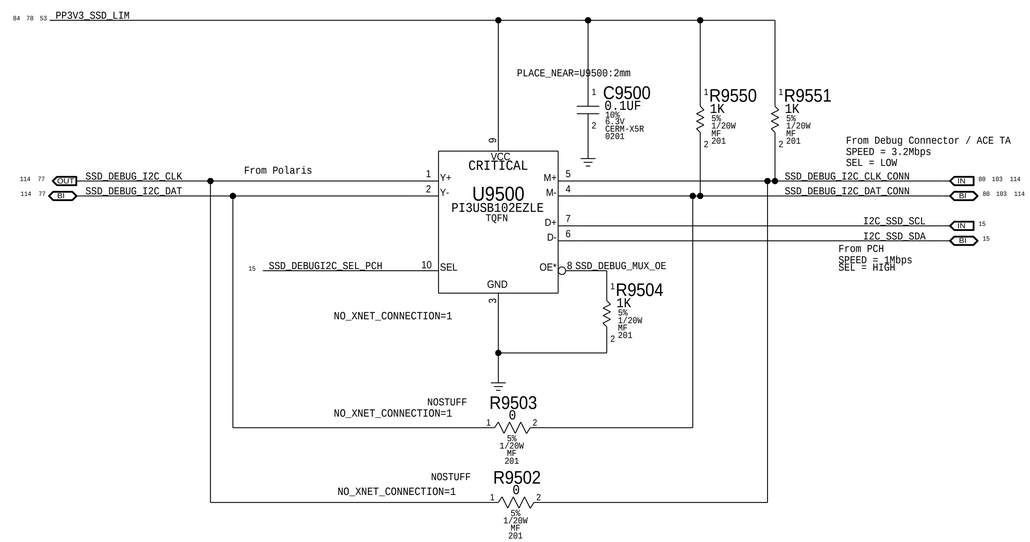

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PAGE TITLE
SSD SUPPORT

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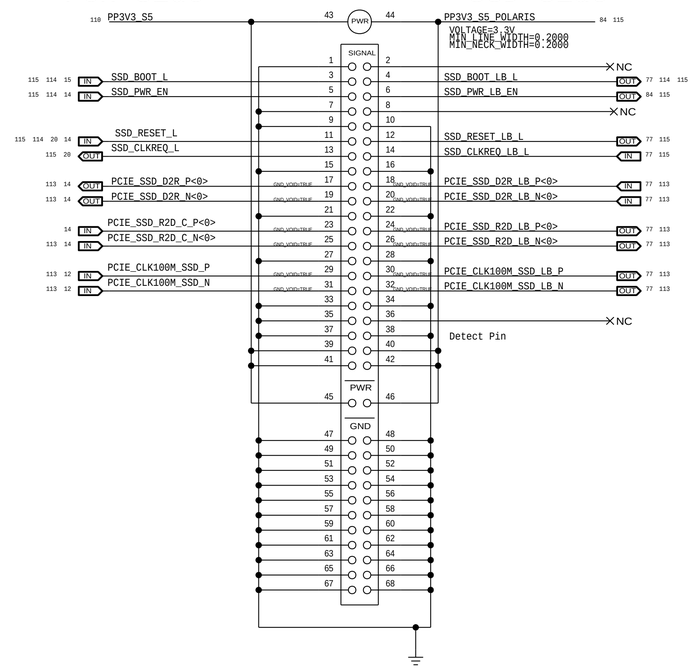
LIFEBOAT

J9600
20759-042E-02
F-ST-SM

PCH Side

SSD Side



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PAGE TITLE
Lifeboat

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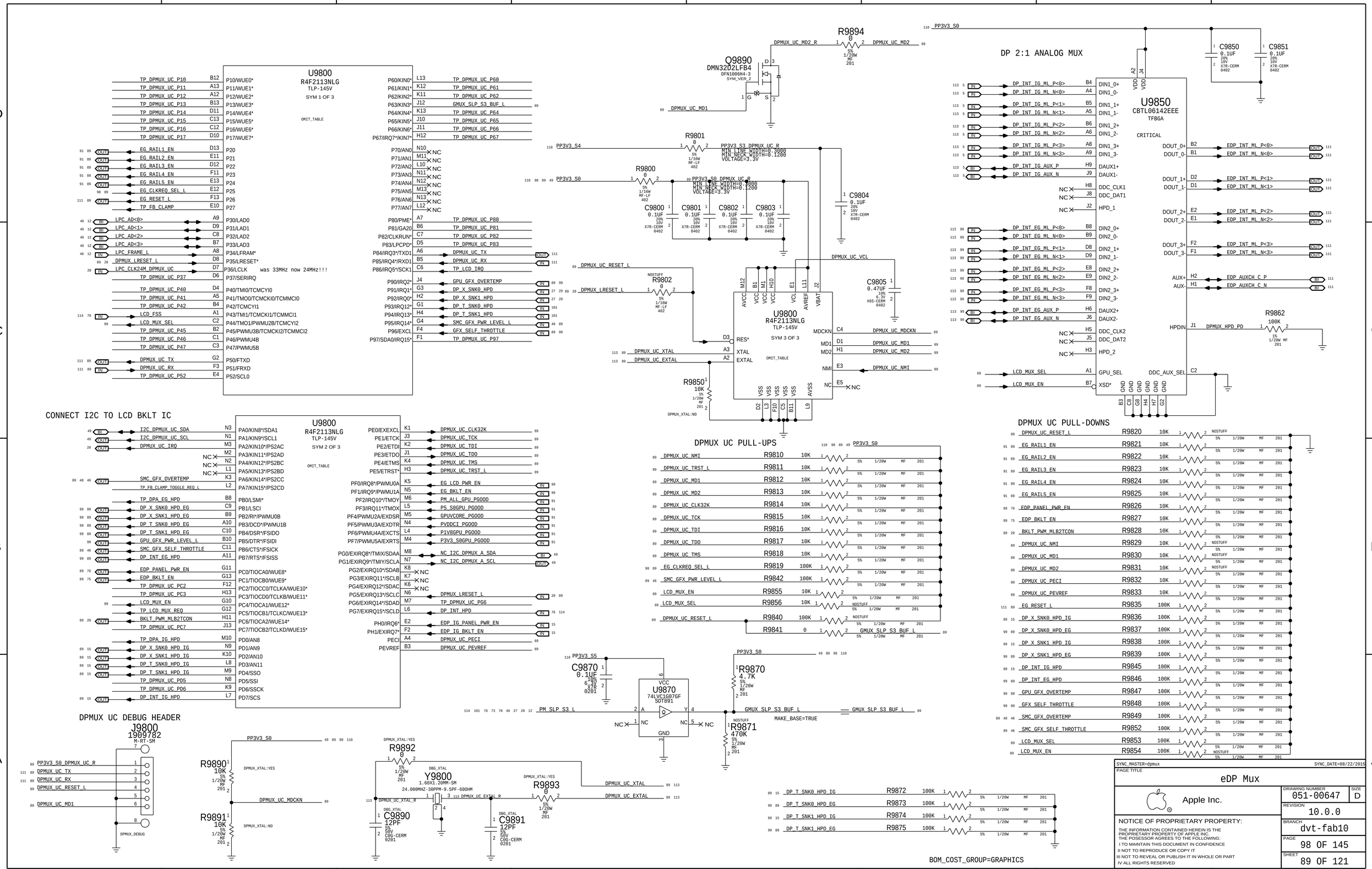
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TLP-145V
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U9800
R4F2113NLG
TLP-145V
SYM 3 OF 3
OMIT_TABLE
Q9890
DMN32D2LFB4
DFN1006H4-3
SYM_VER_2
R9894
DPMUX_UC_MD2_R
DPMUX_UC_MD2
DPMUX_UC_MD1
R9801
PP3V3_S4
PP3V3_S3_DPMUX_UC_R
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DPMUX_UC_RESET_L
R9802
DPMUX_UC_LRESET_L
DPMUX_UC_XTAL
DPMUX_UC_EXTAL
R9850
10K
DPMUX_XTAL:NO
DPMUX_UC_MDCKN
DPMUX_UC_MD1
DPMUX_UC_MD2
DPMUX_UC_NMI
DPMUX UC PULL-UPS
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U9850
CBTL06142EEE
TFBGA
CRITICAL
C9850 0.1UF
C9851 0.1UF
R9862
100K
DPMUX_HPD_PD
DPMUX UC PULL-DOWNS
CONNECT I2C TO LCD BKLT IC
DPMUX UC DEBUG HEADER
J9800
1909782
M-RT-SM
DPMUX_DEBUG
R9890
10K
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DPMUX_UC_MDCKN
R9891
10K
DPMUX_XTAL:NO
R9892
0
DPMUX_XTAL:YES
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24.000MHZ-30PPM-9.5PF-60OHM
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DPMUX_UC_EXTAL_R
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C9891
12PF
R9893
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DPMUX_UC_EXTAL
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SYNC_DATE=08/22/2015
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Apple Inc.
DRAWING NUMBER
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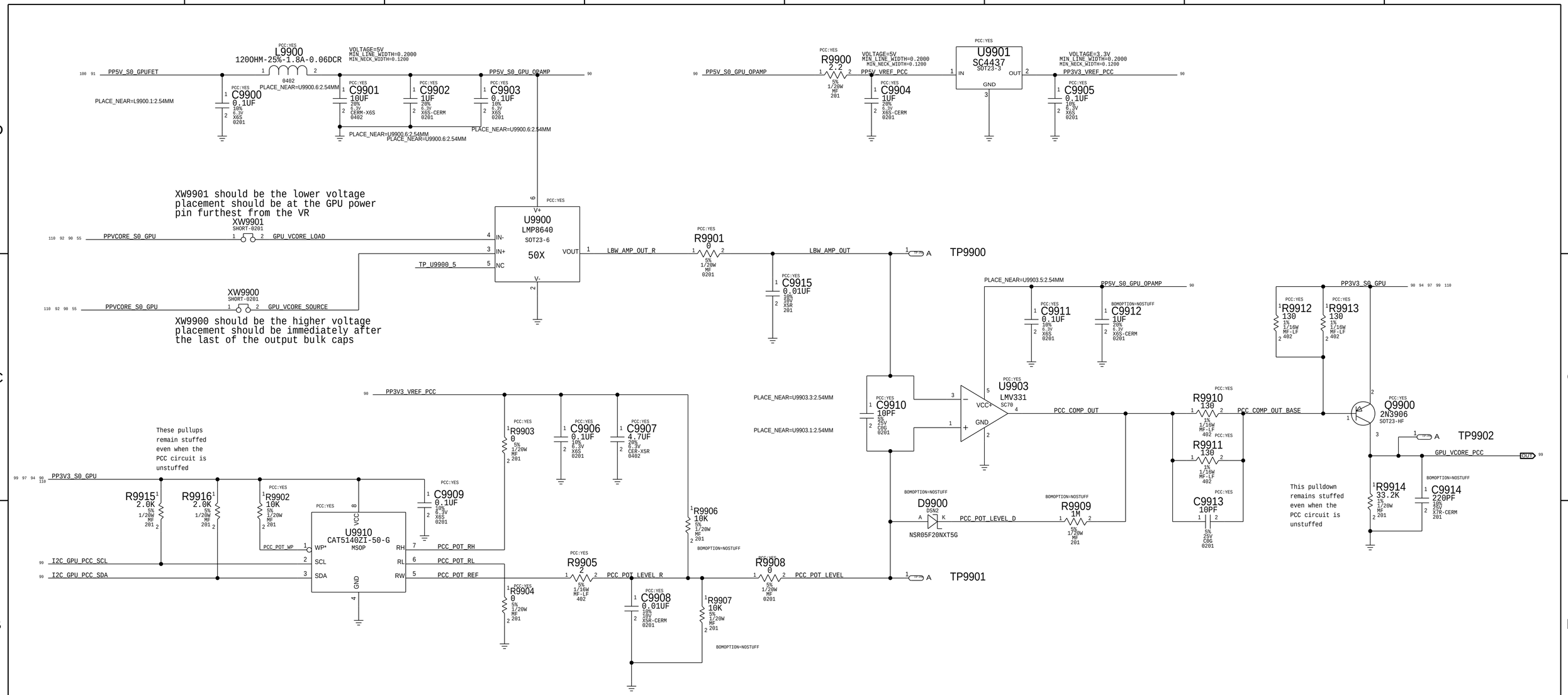

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GPU PCC

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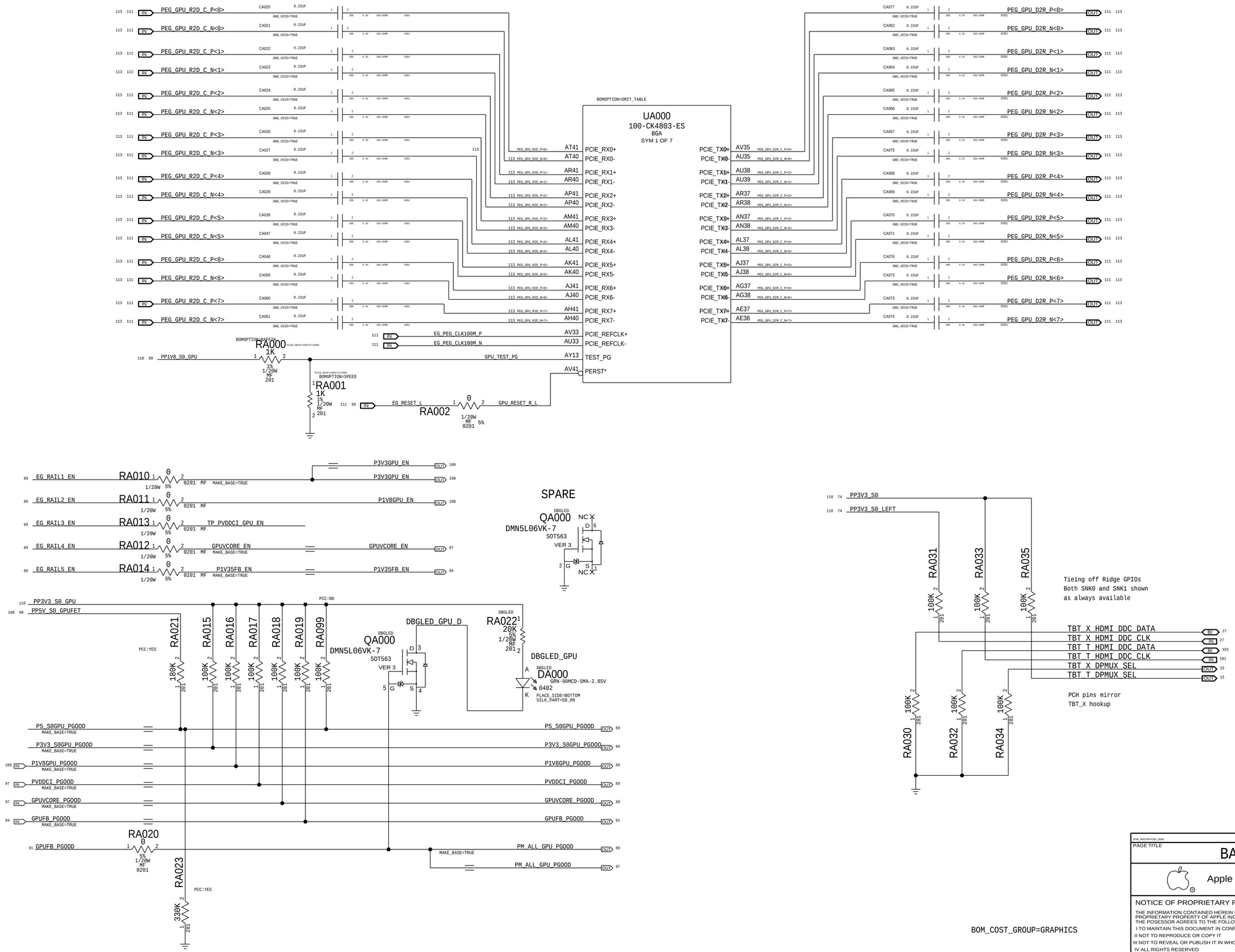

PAGE TITLE

BAFFIN PCI-E

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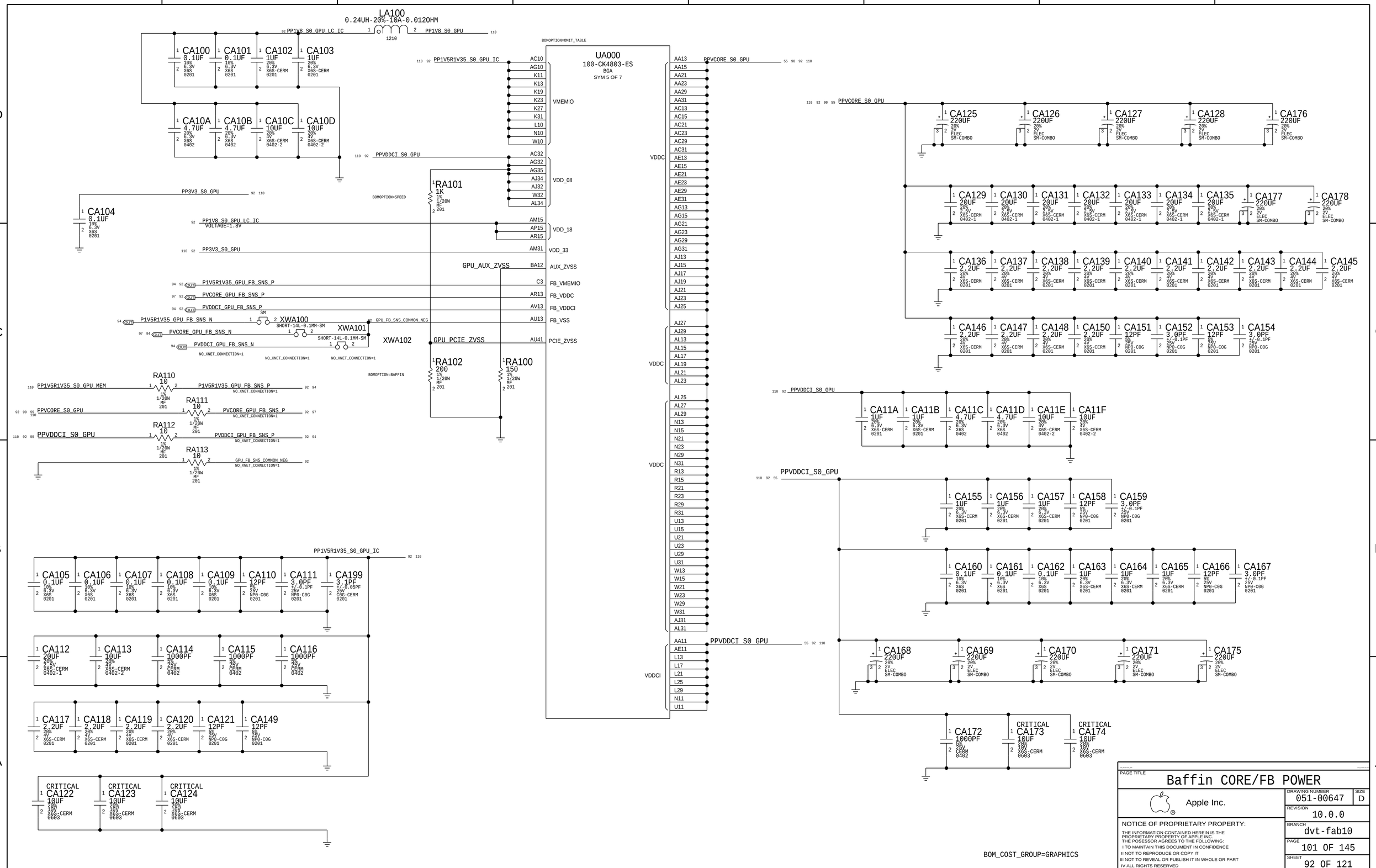

PAGE TITLE

Baffin CORE/FB POWER

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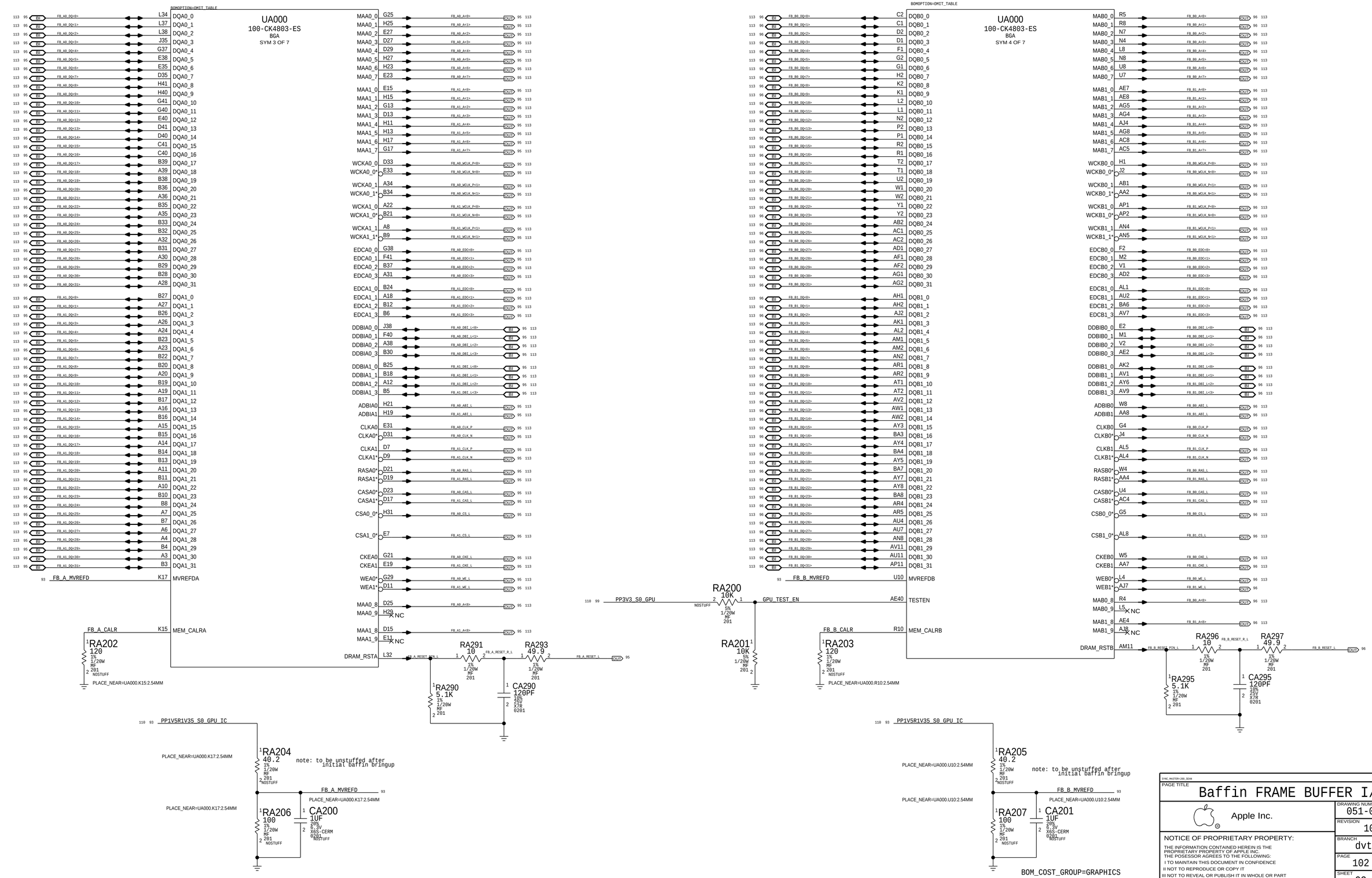

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PAGE TITLE

Baffin FRAME BUFFER I/F

Apple Inc.

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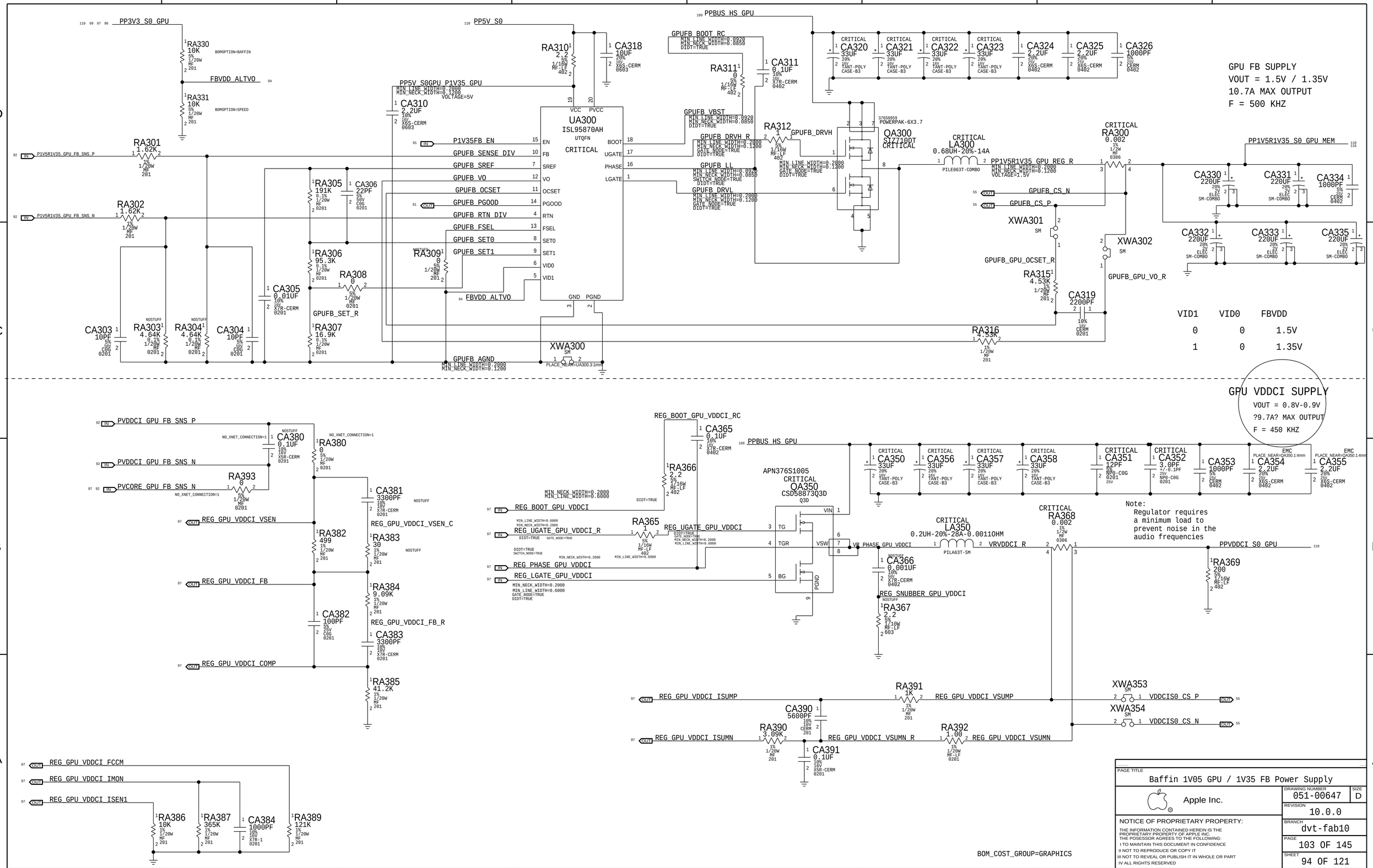

PAGE TITLE
Baffin 1V05 GPU / 1V35 FB Power Supply

Apple Inc.

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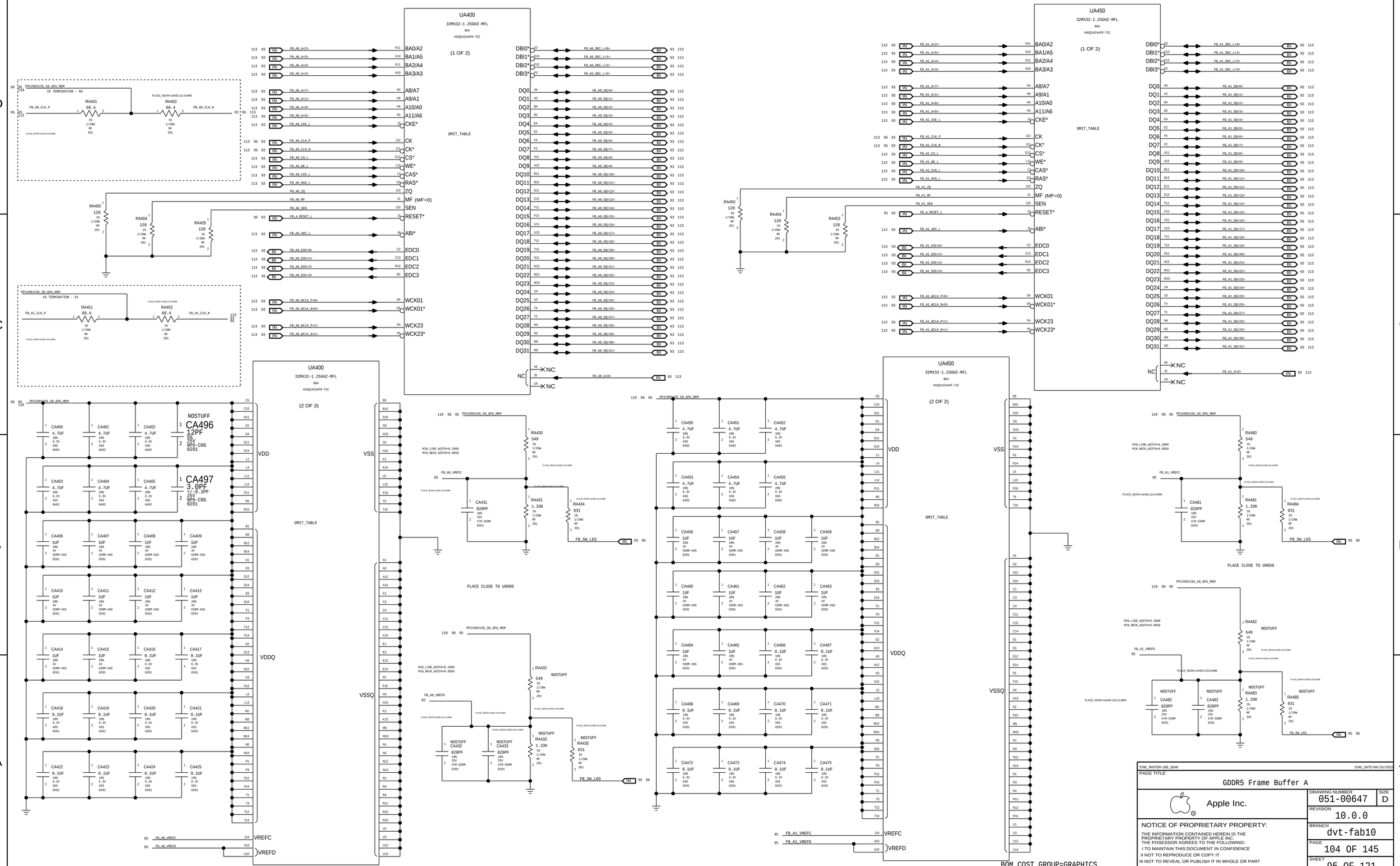
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VDDQ
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VSSQ
VREFC
VREFD
PLACE CLOSE TO U9000
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SYNC_MASTER=J80_SEAN
SYNC_DATE=04/29/2015
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GDDR5 Frame Buffer A
Apple Inc.
DRAWING NUMBER
051-00647
SIZE
D
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BRANCH
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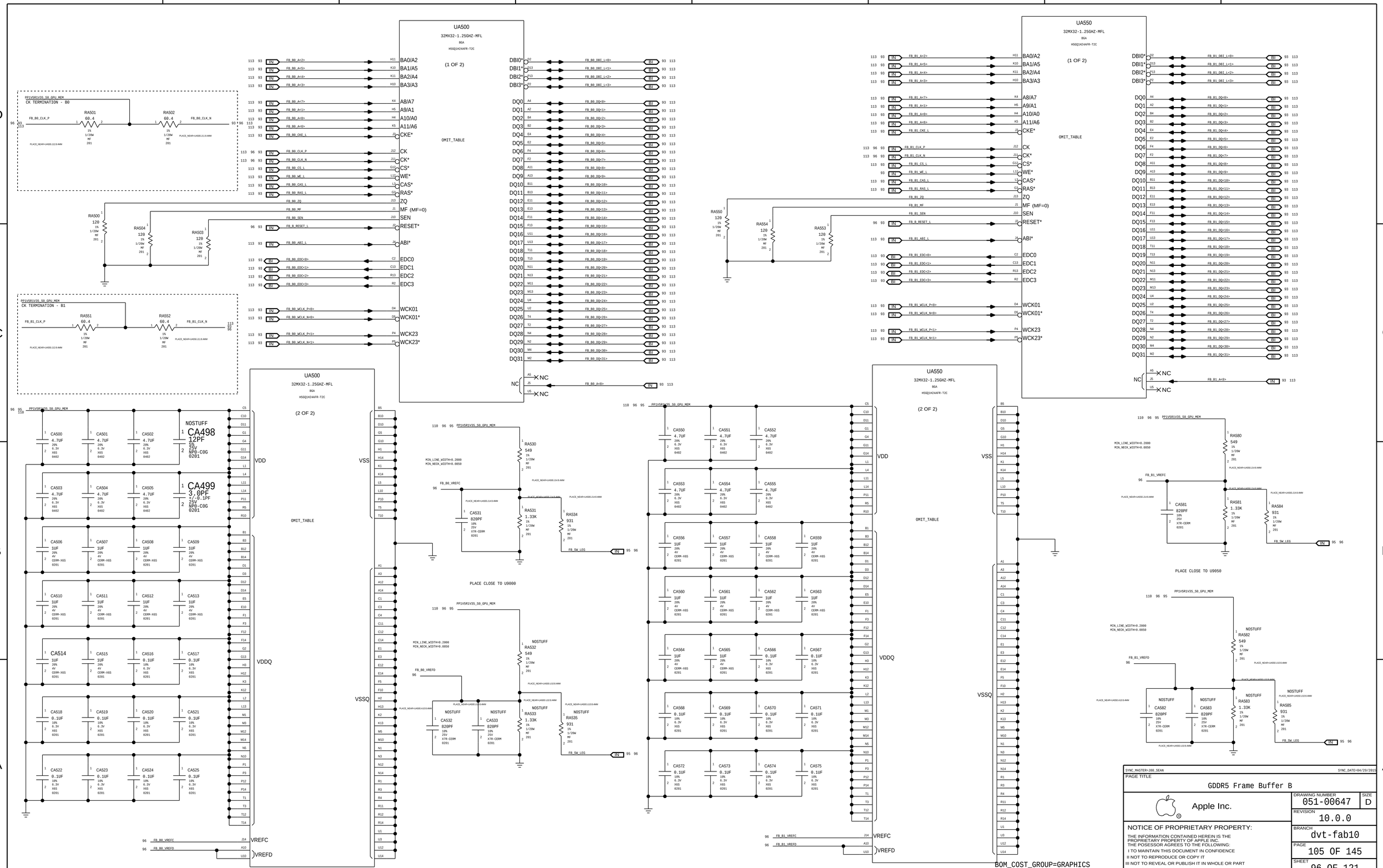

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PAGE TITLE

GDDR5 Frame Buffer B

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
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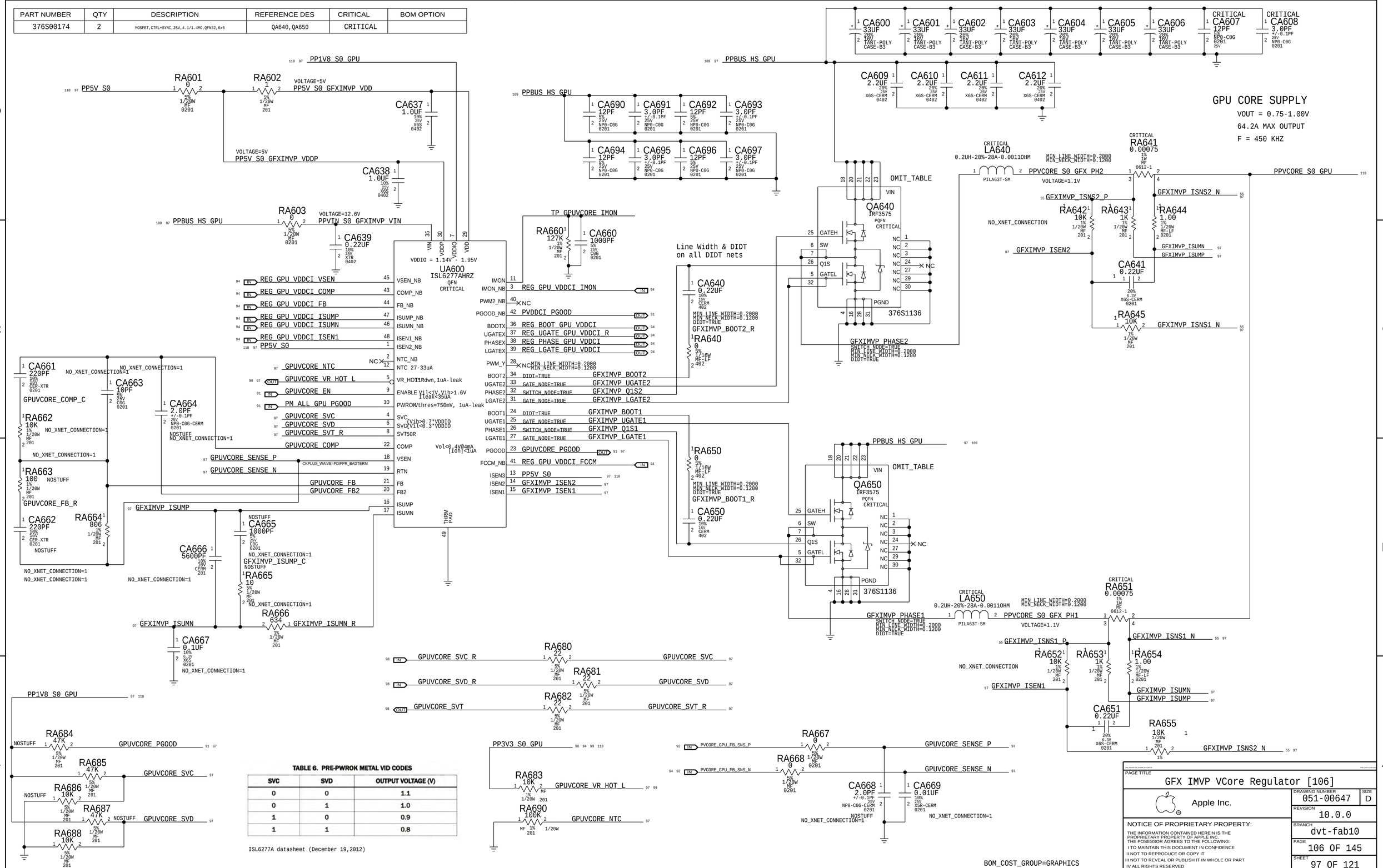

TABLE 6. PRE-PWROK METAL VID CODES

SVC	SVD	OUTPUT VOLTAGE (V)
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0	1	1.0
1	0	0.9
1	1	0.8

ISL6277A datasheet (December 19,2012)

PAGE TITLE
GFX IMVP VCore Regulator [106]

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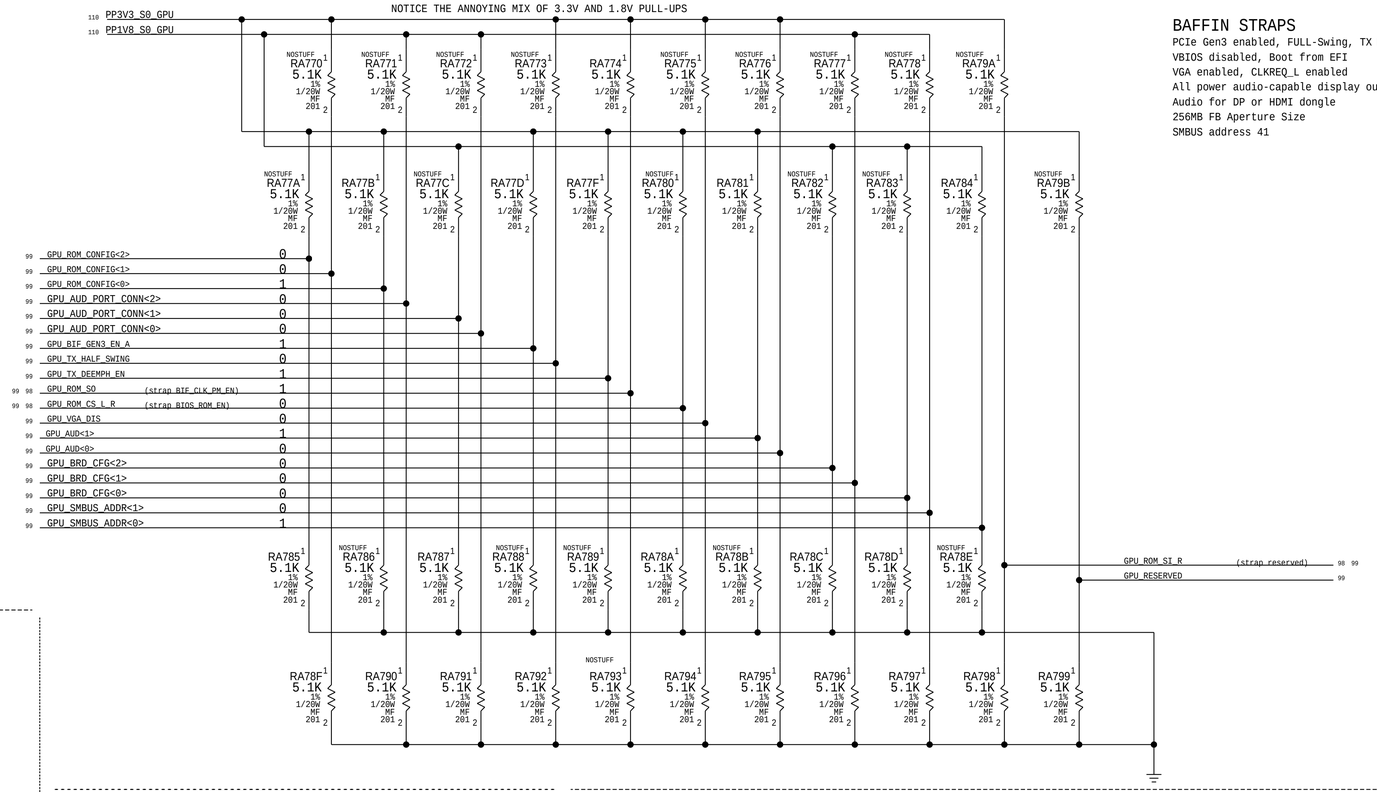
former site of the SPEED MLPS STRAPS

PCIe Gen3 enabled, Half-Swing, TX De-emp enabled
VBIOS disabled, Boot from EFI
VGA enabled
All power audio-capable display output
256MB FB Aperture Size

PS_0:	01001	82nF	8.45k	2k
PS_1:	10001	10nF	8.45k	2k
PS_2:	10000	10nF	NC	4.75k
PS_3:	00000	680nF	NC	4.75k

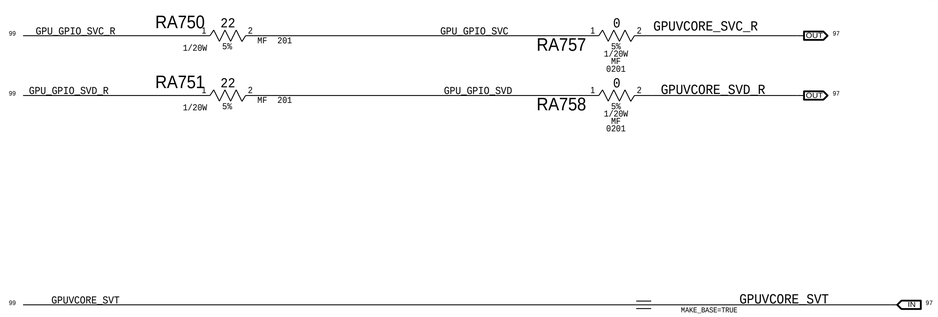
NOTICE THE ANNOYING MIX OF 3.3V AND 1.8V PULL-UPS



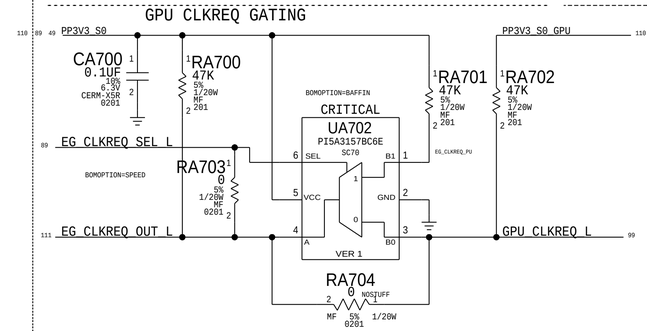
BAFFIN STRAPS

PCIe Gen3 enabled, FULL-Swing, TX De-emp enabled
VBIOS disabled, Boot from EFI
VGA enabled, CLKREQ_L enabled
All power audio-capable display output
Audio for DP or HDMI dongle
256MB FB Aperture Size
SMBUS address 41

Former site of the GPU SVI2 VOLTAGE TRANSLATION SPEED ONLY

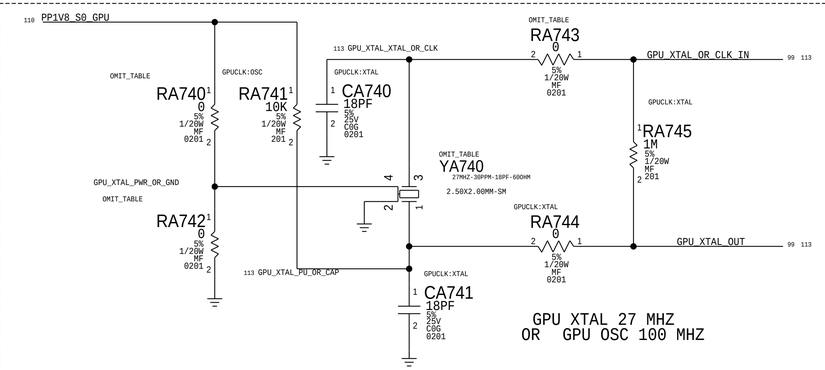


GPU CLKREQ GATING



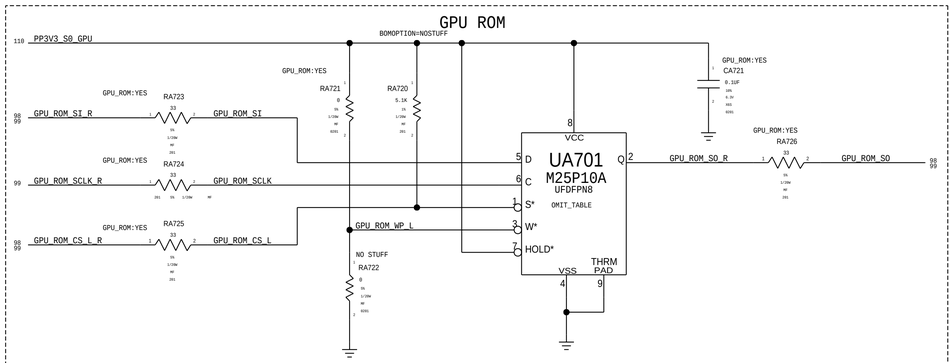
SEL = 0 : PCH CLKREQ CONNECTED TO GPU
SEL = 1 : PCH CLKREQ TIED TO PULLUP

GPU XTAL 27 MHZ OR GPU OSC 100 MHZ

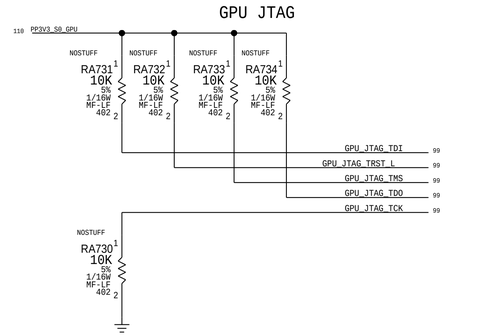


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
197S0499	1	XTAL,27.000MHZ,30PPM,12PF,2.5x2.0MM	YA740	CRITICAL	GPUCLK:XTAL
197S00056	1	OSC,MEMS,100MHZ,+/-20PPM,1.8V,2520	YA740	CRITICAL	GPUCLK:OSC
117S0201	1	RES,0 OHM,5%,0201	RA743	CRITICAL	GPUCLK:XTAL
117S0080	1	RES,33 OHM,5%,0201	RA743	CRITICAL	GPUCLK:OSC
155S0387	1	FERRITE BEAD, 4700HM,0.1A,1.5MOHM DCR,060	RA740	CRITICAL	GPUCLK:OSC
117S0201	1	RES,0 OHM,5%,0201	RA742	CRITICAL	GPUCLK:XTAL
132S0444	1	CAP,CER,X5R,0.1UF,10%,6.3V,0201	RA742	CRITICAL	GPUCLK:OSC

GPU ROM



GPU JTAG



BOM_COST_GROUP=GRAPHICS

PAGE TITLE
Baffin GPIOs,CLK & Straps

Apple Inc.

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REVISION 10.0.0
BRANCH dvt-fab10
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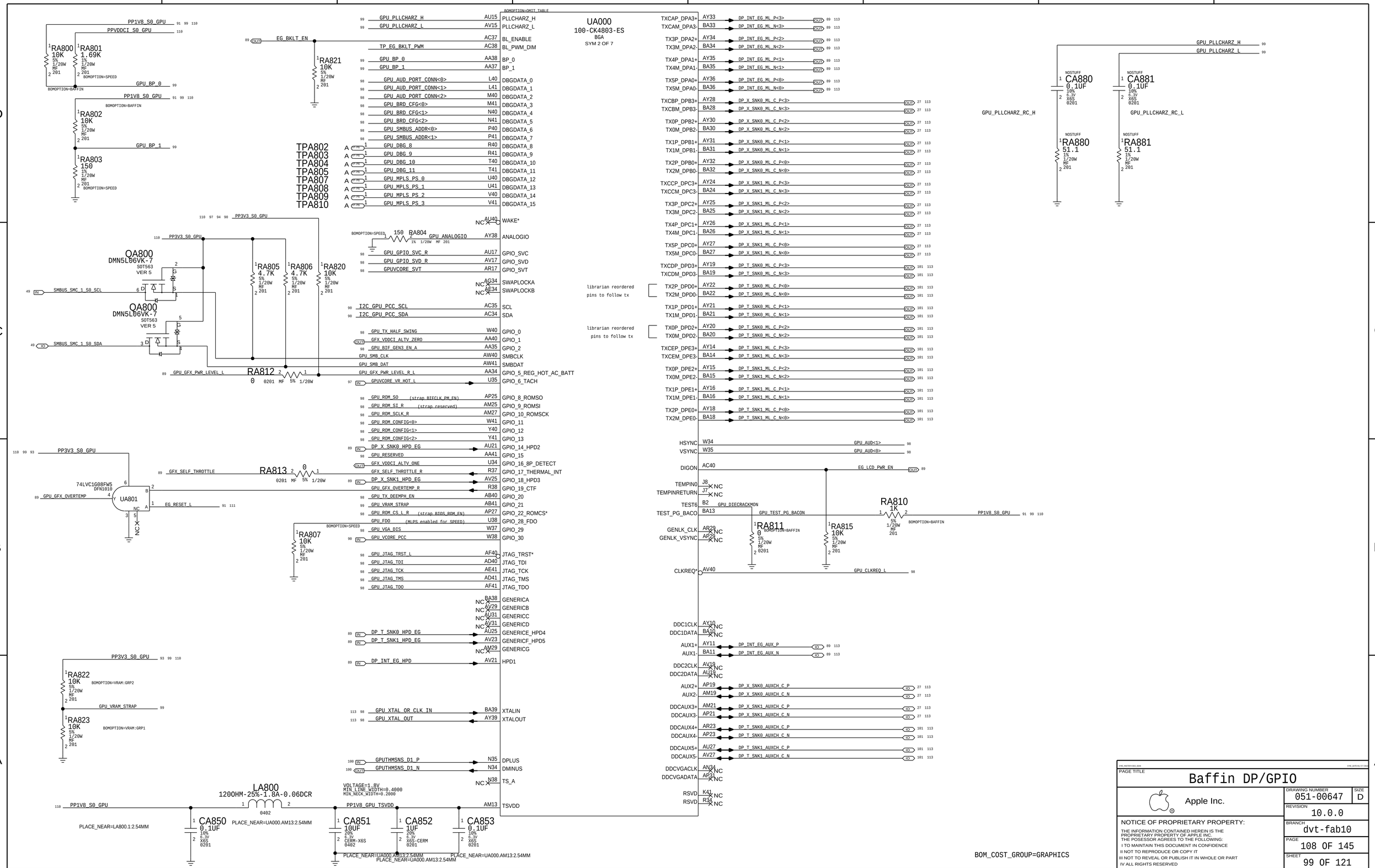
UA000
100-CK4803-ES
BGA
SYM 2 OF 7
PP1V8_S0_GPU
PPVDDCI_S0_GPU
RA800 10K
RA801 1.69K
BOMOPTION=SPEED
BOMOPTION=BAFFIN
RA802 10K
RA803 150
EG_BKLT_EN
RA821 10K
TPA802
TPA803
TPA804
TPA805
TPA807
TPA808
TPA809
TPA810
PLLCHARZ_H
PLLCHARZ_L
BL_ENABLE
BL_PWM_DIM
BP_0
BP_1
DBGDATA_0
DBGDATA_1
DBGDATA_2
DBGDATA_3
DBGDATA_4
DBGDATA_5
DBGDATA_6
DBGDATA_7
DBGDATA_8
DBGDATA_9
DBGDATA_10
DBGDATA_11
DBGDATA_12
DBGDATA_13
DBGDATA_14
DBGDATA_15
WAKE*
ANALOGIO
GPIO_SVC
GPIO_SVD
GPIO_SVT
SWAPLOCKA
SWAPLOCKB
SCL
SDA
GPIO_0
GPIO_1
GPIO_2
SMBCLK
SMBDAT
GPIO_5_REG_HOT_AC_BATT
GPIO_6_TACH
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_11
GPIO_12
GPIO_13
GPIO_14_HPD2
GPIO_15
GPIO_16_8P_DETECT
GPIO_17_THERMAL_INT
GPIO_18_HPD3
GPIO_19_CTF
GPIO_20
GPIO_21
GPIO_22_ROMCS*
GPIO_28_FDO
GPIO_29
GPIO_30
JTAG_TRST*
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
GENERICA
GENERICB
GENERICC
GENERICD
GENERICE_HPD4
GENERICF_HPD5
GENERICG
HPD1
XTALIN
XTALOUT
DPLUS
DMINUS
TS_A
TSVDD
QA800
DMN5L06VK-7
SOT563
VER 5
RA805 4.7K
RA806 4.7K
RA820 10K
SMBUS_SMC_1_S0_SCL
SMBUS_SMC_1_S0_SDA
RA804 150
RA812 0
GPU_GFX_PWR_LEVEL_L
RA813 0
GPU_GFX_SELF_THROTTLE
GPU_GFX_OVERTEMP
EG_RESET_L
74LVC1G08FW5
DFN1010
UA801
RA807 10K
RA822 10K
RA823 10K
GPU_VRAM_STRAP
LA800
120OHM-25%-1.8A-0.06DCR
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.2000
CA850 0.1UF
CA851 10UF
CA852 1UF
CA853 0.1UF
PLACE_NEAR=LA800.1:2.54MM
PLACE_NEAR=UA000.AM13:2.54MM
TXCAP_DPA3+
TXCAM_DPA3-
TX3P_DPA2+
TX3M_DPA2-
TX4P_DPA1+
TX4M_DPA1-
TX5P_DPA0+
TX5M_DPA0-
TXCBP_DPB3+
TXCBM_DPB3-
TX0P_DPB2+
TX0M_DPB2-
TX1P_DPB1+
TX1M_DPB1-
TX2P_DPB0+
TX2M_DPB0-
TXCCP_DPC3+
TXCCM_DPC3-
TX3P_DPC2+
TX3M_DPC2-
TX4P_DPC1+
TX4M_DPC1-
TX5P_DPC0+
TX5M_DPC0-
TXCDP_DPD3+
TXCDM_DPD3-
TX2P_DPD0+
TX2M_DPD0-
TX1P_DPD1+
TX1M_DPD1-
TX0P_DPD2+
TX0M_DPD2-
TXCEP_DPE3+
TXCEM_DPE3-
TX0P_DPE2+
TX0M_DPE2-
TX1P_DPE1+
TX1M_DPE1-
TX2P_DPE0+
TX2M_DPE0-
librarian reordered pins to follow tx
HSYNC
VSYNC
DIGON
TEMPIN0
TEMPINRETURN
TEST6
TEST_PG_BACO
GENLK_CLK
GENLK_VSYNC
CLKREQ*
RA811 0
RA815 10K
RA810 1K
GPU_TEST_PG_BACON
GPU_DIECRACKMON
GPU_CLKREQ_L
EG_LCD_PWR_EN
DDC1CLK
DDC1DATA
AUX1+
AUX1-
DDC2CLK
DDC2DATA
AUX2+
AUX2-
DDCAUX3+
DDCAUX3-
DDCAUX4+
DDCAUX4-
DDCAUX5+
DDCAUX5-
DDCVGACLK
DDCVGADATA
RSVD
GPU_PLLCHARZ_RC_H
GPU_PLLCHARZ_RC_L
CA880 0.1UF
CA881 0.1UF
RA880 51.1
RA881 51.1
BOM_COST_GROUP=GRAPHICS
PAGE TITLE
Baffin DP/GPIO
Apple Inc.
DRAWING NUMBER
051-00647
SIZE
D
REVISION
10.0.0
BRANCH
dvt-fab10
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99 OF 121
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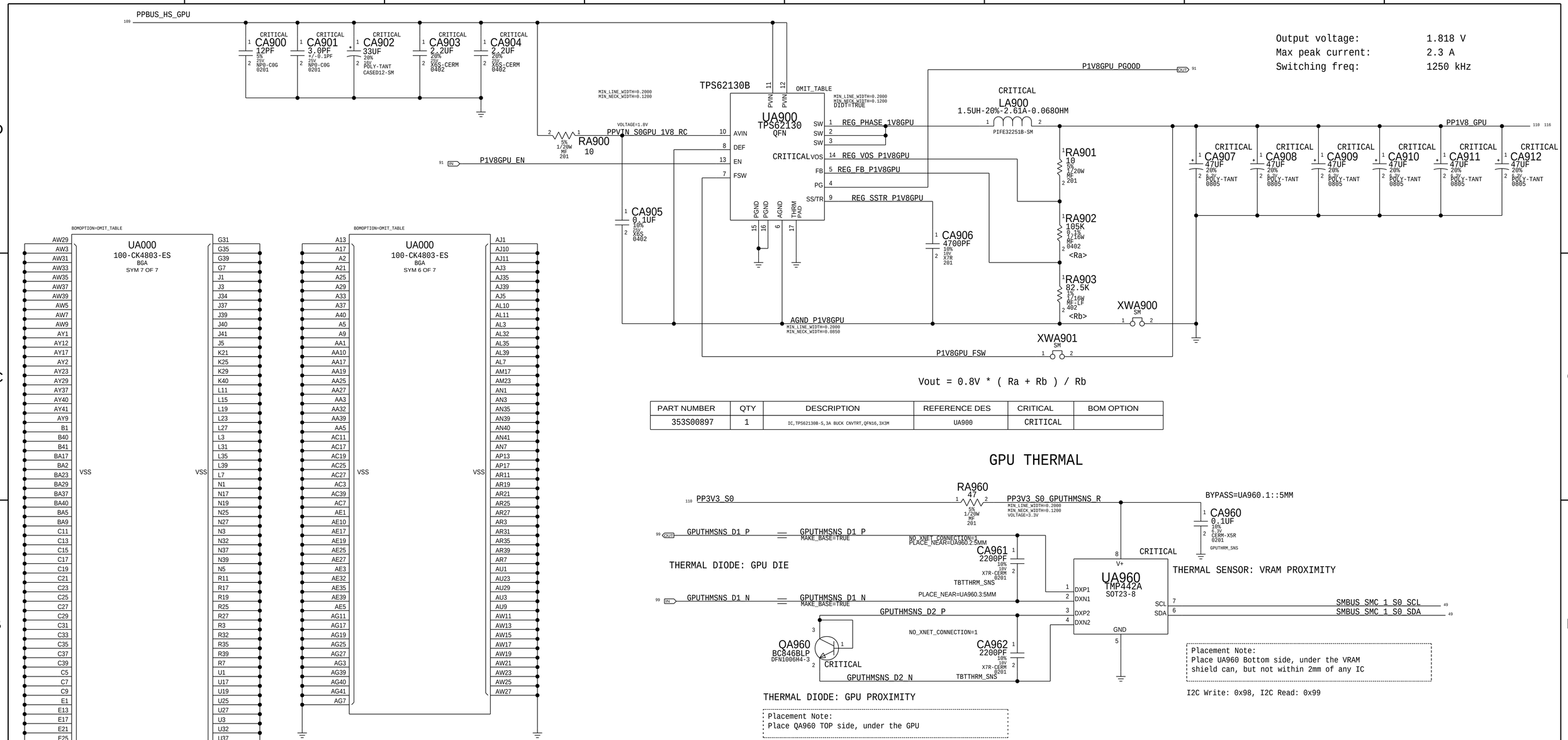


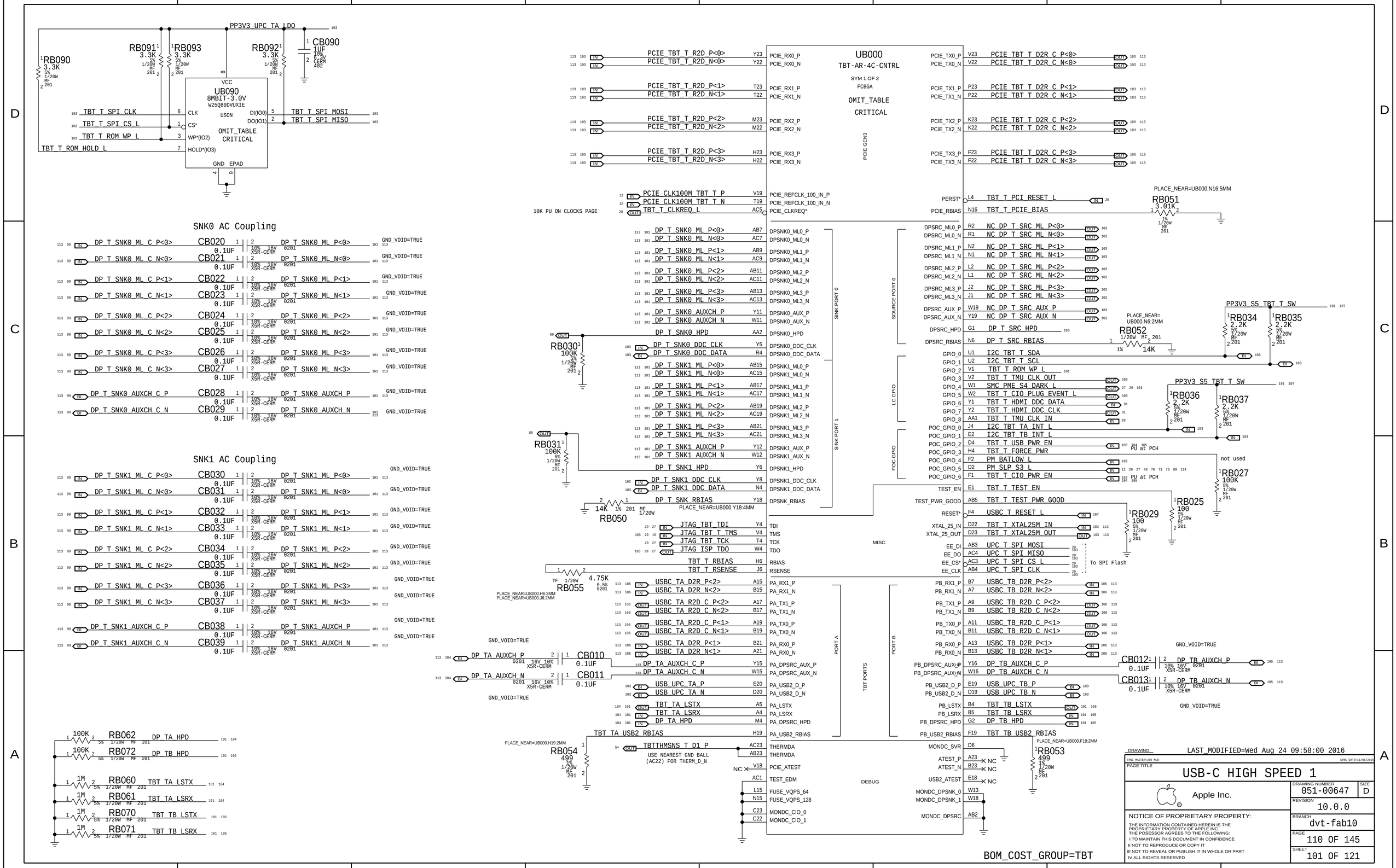
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00897	1	IC,TPS62130B-S,3A BUCK CNVTRT,QFN16,3X3M	UA900	CRITICAL	

UA950

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

UA951

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max


PP3V3_UPC_TA_LDO
RB090 3.3K 5% 1/20W MF 201
RB091 3.3K 5% 1/20W MF 201
RB093 3.3K 5% 1/20W MF 201
RB092 3.3K 5% 1/20W MF 201
CB090 1UF 10% 6.3V X5R-CERM 402
UB090 8MBIT-3.0V W25Q80DVUXIE USON
OMIT_TABLE CRITICAL
TBT_T_SPI_CLK
TBT_T_SPI_CS_L
TBT_T_ROM_WP_L
TBT_T_ROM_HOLD_L
TBT_T_SPI_MOSI
TBT_T_SPI_MISO
SNK0 AC Coupling
SNK1 AC Coupling
UB000 TBT-AR-4C-CNTRL
SYM 1 OF 2 FCBGA
OMIT_TABLE CRITICAL
PCIE GEN3
10K PU ON CLOCKS PAGE
PLACE_NEAR=UB000.N16:5MM
RB051 3.01K 1% 1/20W MF 201
PLACE_NEAR=UB000.N6:2MM
RB052 14K 1% 1/20W MF 201
RB030 100K 5% 1/20W MF 201
RB031 100K 5% 1/20W MF 201
RB050 14K 1% 201 MF 1/20W
PLACE_NEAR=UB000.Y18:4MM
RB055 4.75K 0.5% 0201
PLACE_NEAR=UB000.H6:2MM
PLACE_NEAR=UB000.J6:2MM
RB054 499 1% 1/20W MF 201
PLACE_NEAR=UB000.H19:2MM
RB053 499 1% 1/20W MF 201
PLACE_NEAR=UB000.F19:2MM
RB034 2.2K 5% 1/20W MF 201
RB035 2.2K 5% 1/20W MF 201
RB036 2.2K 5% 1/20W MF 201
RB037 2.2K 5% 1/20W MF 201
RB027 100K 5% 1/20W MF 201
RB025 100 5% 1/20W MF 201
RB029 100 5% 1/20W MF 201
PP3V3_S5_TBT_T_SW
not used
PU at PCH
To SPI Flash
SINK PORT 0
SINK PORT 1
SOURCE PORT 0
LC GPIO
POC GPIO
MISC
TBT PORTS
PORT A
PORT B
DEBUG
USB_UPC_TA_P
USB_UPC_TA_N
USB_UPC_TB_P
USB_UPC_TB_N
USE NEAREST GND BALL (AC22) FOR THERM_D_N
RB062 100K DP_TA_HPD
RB072 100K DP_TB_HPD
RB060 1M TBT_TA_LSTX
RB061 1M TBT_TA_LSRX
RB070 1M TBT_TB_LSTX
RB071 1M TBT_TB_LSRX
BOM_COST_GROUP=TBT
DRAWING
LAST_MODIFIED=Wed Aug 24 09:58:00 2016
PAGE TITLE
USB-C HIGH SPEED 1
Apple Inc.
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
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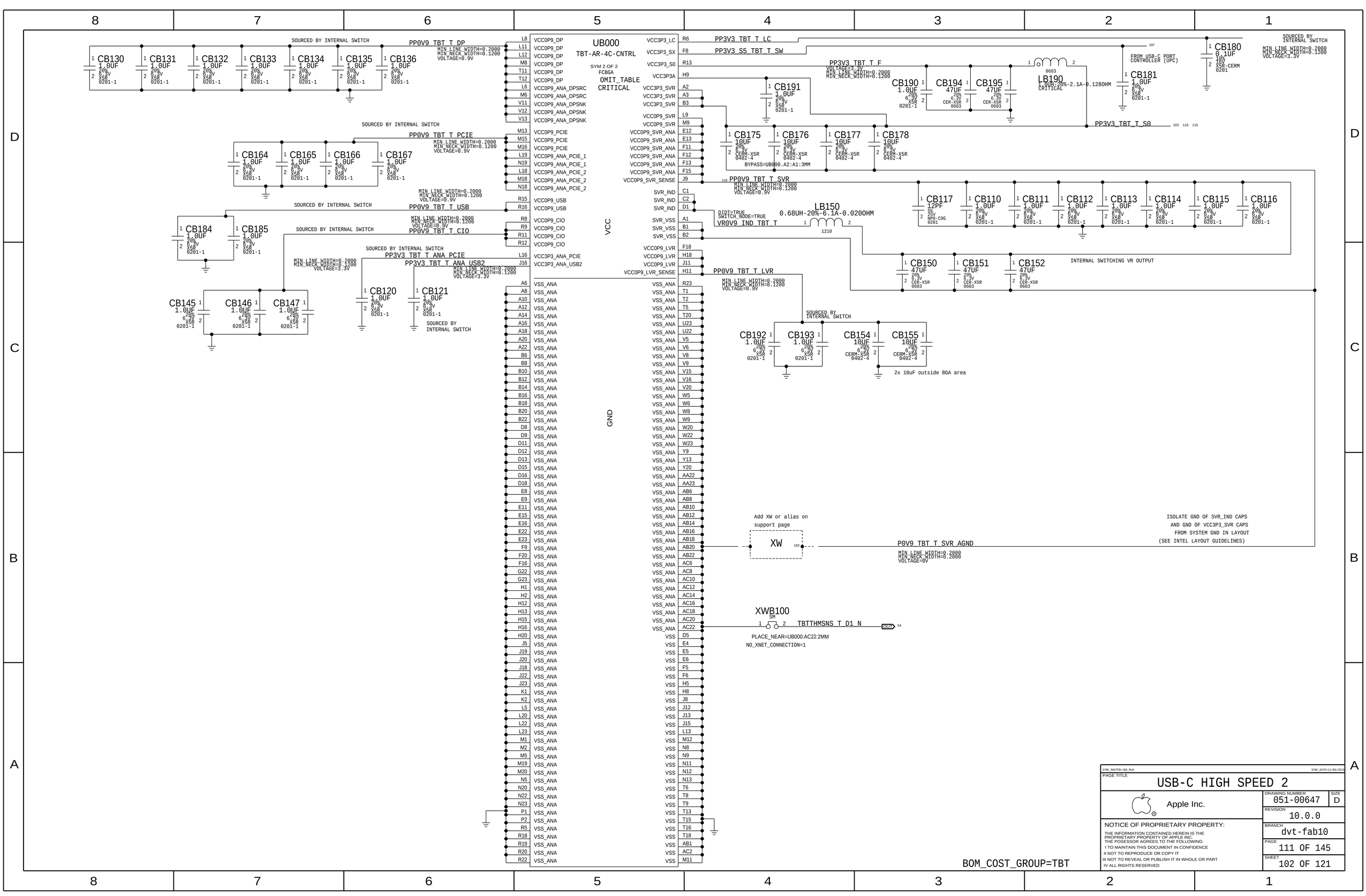
UB000
TBT-AR-4C-CNTRL
SYM 2 OF 2
FCBGA
OMIT_TABLE
CRITICAL
VCC
GND
SOURCED BY INTERNAL SWITCH
PP0V9_TBT_T_DP
PP0V9_TBT_T_PCIE
PP0V9_TBT_T_USB
PP0V9_TBT_T_CIO
PP3V3_TBT_T_ANA_PCIE
PP3V3_TBT_T_ANA_USB2
PP3V3_TBT_T_LC
PP3V3_S5_TBT_T_SW
PP3V3_TBT_T_F
PP3V3_TBT_T_S0
PP0V9_TBT_T_SVR
VR0V9_IND_TBT_T
PP0V9_TBT_T_LVR
P0V9_TBT_T_SVR_AGND
TBTTHMSNS_T_D1_N
FROM USB-C PORT CONTROLLER (UPC)
INTERNAL SWITCHING VR OUTPUT
2x 10uF outside BGA area
Add XW or alias on support page
ISOLATE GND OF SVR_IND CAPS AND GND OF VCC3P3_SVR CAPS FROM SYSTEM GND IN LAYOUT (SEE INTEL LAYOUT GUIDELINES)
BYPASS=UB000.A2:A1:3MM
PLACE_NEAR=UB000.AC22:2MM
NO_XNET_CONNECTION=1
BOM_COST_GROUP=TBT
USB-C HIGH SPEED 2
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TMU CLKs

TBT_T_TMU_CLK_OUT — MAKE_BASE=TRUE — TBT_T_TMU_CLK_OUT
RB225 15 (5% 1/20W MF 201) PLACE_NEAR=UB000.V2:5mm
TBT_X_TMU_CLK_IN — MAKE_BASE=TRUE — TBT_X_TMU_CLK_IN
RB226 100K (5% 1/20W MF 201)

DP SRC OPTIONS

IF DP SRC NOT USED

DP_T_SRC_HPD — RB240 1M (5% 1/20W MF 201)

NC_DP_T_SRC_ML_P<3..0>	NC_DP_T_SRC_ML_P<3..0>	MAKE_BASE=TRUE
NC_DP_T_SRC_ML_N<3..0>	NC_DP_T_SRC_ML_N<3..0>	MAKE_BASE=TRUE, NO_TEST=1
NC_DP_T_SRC_AUX_P	NC_DP_T_SRC_AUX_P	MAKE_BASE=TRUE
NC_DP_T_SRC_AUX_N	NC_DP_T_SRC_AUX_N	MAKE_BASE=TRUE

FUSES FOR UPC

PP20V_USBC_TA_VBUS — FB200 (PLACE_NEAR=QB300:5MM, CRITICAL, 0603, 6AMP-32V-0.0095OHM) — PP20V_USBC_TA_VBUS_F
PP20V_USBC_TB_VBUS — FB201 (PLACE_NEAR=QB400:5MM, CRITICAL, 0603, 740S0135, 6AMP-32V-0.0095OHM) — PP20V_USBC_TB_VBUS_F

25MHz xtal

TBT_T_XTAL25M_OUT — RB207 0 (5% 1/20W MF 201) — TBT_T_XTAL25M_OUT_R
NOSTUFF RB206 1M (5% 1/20W MF 201)
to/from Ridge
CRITICAL YB200 25MHZ-25PPM-20PF-50HM 2.00X1.60-SM
CB202 20PF (5% 25V C0G 0201)
CB203 20PF (5% 25V C0G 0201)
TBT_T_XTAL25M_IN

AR/ACE SPI BUS SERIES R'S

ROM: TBT_T_SPI_CLK, TBT_T_SPI_CS_L, TBT_T_SPI_MOSI, TBT_T_SPI_MISO

RB290 100	TBT_T_SPI_CLK_DBG		
RB280 15	UPC_TA_SPI_CLK	IN	Ace
RB281 15	UPC_TA_SPI_CS_L	IN	Ace
RB282 15	UPC_TA_SPI_MOSI	IN	Ace
RB283 15	UPC_TA_SPI_MISO	OUT	Ace
RB284 15	UPC_T_SPI_CLK	IN	AR
RB285 15	UPC_T_SPI_CS_L	IN	AR
RB286 15	UPC_T_SPI_MOSI	IN	AR
RB287 15	UPC_T_SPI_MISO	OUT	AR

(5% 1/20W MF 201)

TBT to ACE

TBT — Alpine Ridge U2800 (MASTER)

MAKE_BASE=TRUE	I2C_TBT_T_SCL	I2C_TBT_T_SCL
MAKE_BASE=TRUE	I2C_TBT_T_SDA	I2C_TBT_T_SDA
MAKE_BASE=TRUE	I2C_TBT_TA_INT_L	I2C_TBT_TA_INT_L
MAKE_BASE=TRUE	I2C_TBT_TB_INT_L	I2C_TBT_TB_INT_L

Pri ACE — U3100 (Write: 0x70 Read: 0x71)

Sec ACE — U3200 (Write: 0x7E Read: 0x7F)

I2C_TBT_T_SCL, I2C_TBT_T_SDA, I2C_TBT_TB_INT_L

Ridge PCIE Caps

R2D

PCIE_TBT_T_R2D_C_P<0>	CB240 0.22UF	PCIE_TBT_T_R2D_P<0>	GND_VOID=TRUE
PCIE_TBT_T_R2D_C_N<0>	CB241 0.22UF	PCIE_TBT_T_R2D_N<0>	GND_VOID=TRUE
PCIE_TBT_T_R2D_C_P<1>	CB242 0.22UF	PCIE_TBT_T_R2D_P<1>	GND_VOID=TRUE
PCIE_TBT_T_R2D_C_N<1>	CB243 0.22UF	PCIE_TBT_T_R2D_N<1>	GND_VOID=TRUE
PCIE_TBT_T_R2D_C_P<2>	CB244 0.22UF	PCIE_TBT_T_R2D_P<2>	GND_VOID=TRUE
PCIE_TBT_T_R2D_C_N<2>	CB245 0.22UF	PCIE_TBT_T_R2D_N<2>	GND_VOID=TRUE
PCIE_TBT_T_R2D_C_P<3>	CB246 0.22UF	PCIE_TBT_T_R2D_P<3>	GND_VOID=TRUE
PCIE_TBT_T_R2D_C_N<3>	CB247 0.22UF	PCIE_TBT_T_R2D_N<3>	GND_VOID=TRUE

(0201 X5R 6.3V 20%)

D2R

PCIE_TBT_T_D2R_C_P<0>	CB250 0.22UF	PCIE_TBT_T_D2R_P<0>	GND_VOID=TRUE
PCIE_TBT_T_D2R_C_N<0>	CB251 0.22UF	PCIE_TBT_T_D2R_N<0>	GND_VOID=TRUE
PCIE_TBT_T_D2R_C_P<1>	CB252 0.22UF	PCIE_TBT_T_D2R_P<1>	GND_VOID=TRUE
PCIE_TBT_T_D2R_C_N<1>	CB253 0.22UF	PCIE_TBT_T_D2R_N<1>	GND_VOID=TRUE
PCIE_TBT_T_D2R_C_P<2>	CB254 0.22UF	PCIE_TBT_T_D2R_P<2>	GND_VOID=TRUE
PCIE_TBT_T_D2R_C_N<2>	CB255 0.22UF	PCIE_TBT_T_D2R_N<2>	GND_VOID=TRUE
PCIE_TBT_T_D2R_C_P<3>	CB256 0.22UF	PCIE_TBT_T_D2R_P<3>	GND_VOID=TRUE
PCIE_TBT_T_D2R_C_N<3>	CB257 0.22UF	PCIE_TBT_T_D2R_N<3>	GND_VOID=TRUE

(0201 X5R 6.3V 20%)

ACE Debug Support

OMIT RB289 NOSTUFF (NONE NONE NONE NONE 402): TP_UPC_TA_DBG_UART_TX — TP_UPC_TA_DBG_UART_RX
OMIT RB288 NOSTUFF (NONE NONE NONE NONE 402): TP_UPC_TB_DBG_UART_TX — TP_UPC_TB_DBG_UART_RX

TP_UPC_TA_SWD_DATA — TPB201 (TP-P5)
TP_UPC_TA_SWD_CLK — TPB202 (TP-P5)
TP_UPC_TB_SWD_DATA — TPB203 (TP-P5)
TP_UPC_TB_SWD_CLK — TPB204 (TP-P5)

USBC 5V EN PD

UPC_T_5V_EN — RB232 100K (5% 1/20W MF 201)

ACE A/B RPD STRAPPING

USBC_TA_CC1	USBC_TA_CC1	MAKE_BASE=TRUE
USBC_TB_CC1	USBC_TB_CC1	MAKE_BASE=TRUE
USBC_TA_CC2	USBC_TA_CC2	MAKE_BASE=TRUE
USBC_TB_CC2	USBC_TB_CC2	MAKE_BASE=TRUE

Ridge PDs

DP_T_SNK0_DDC_CLK	DP_T_SNK0_DDC_CLK (MAKE_BASE=TRUE)	RB267 100K
DP_T_SNK0_DDC_DATA	DP_T_SNK0_DDC_DATA (MAKE_BASE=TRUE)	RB268 100K
DP_T_SNK1_DDC_CLK	DP_T_SNK1_DDC_CLK (MAKE_BASE=TRUE)	RB269 100K
DP_T_SNK1_DDC_DATA	DP_T_SNK1_DDC_DATA (MAKE_BASE=TRUE)	RB270 100K

(5% 1/20W MF 201)

ACE PDs

UPC_TA_DBG3	RB260 100K
UPC_TA_DBG4	RB261 100K
UPC_TB_DBG3	RB262 100K
UPC_TB_DBG4	RB263 100K
UPC_TA_DBG1	RB264 100K
UPC_TA_DBG2	RB265 100K
UPC_TA_HPD_RX	RB233 100K
UPC_TB_HPD_RX	RB234 100K

(5% 1/20W MF 201)

ACE FET DCIN Bypass Caps

PPDCIN_G3H — CB211, CB212, CB213, CB214 0.1UF (10% 35V CER-X5R 0201)

RIDGE 0.9V SVR XW

XWB200 (SM): P0V9_TBT_T_SVR_AGND — NO_XNET_CONNECTION=1

I2C SERIES R'S

I2C_UPC_T_SDA2 — RB241 33 (5% 1/20W MF 201) — SMBUS_SMC_4_G3H_SDA (PLACE_NEAR=U5000:5mm)
I2C_UPC_T_SCL2 — RB242 33 (5% 1/20W MF 201) — SMBUS_SMC_4_G3H_SCL (PLACE_NEAR=U5000:5mm)

ACE DEBUG CONN

Place on bottom

USBC_DBG — JB200 505070-1220 M-ST-SM

I2C_TBT_TB_INT_L	I2C_TBT_TA_INT_L
I2C_UPC_T_SCL2	I2C_TBT_T_SDA
I2C_UPC_T_SDA2	I2C_TBT_T_SCL
SMC_USBC_INT_L	TBT_T_CIO_PWR_EN
TBT_T_SPI_CLK_DBG	TBT_T_USB_PWR_EN
UPC_TA_UART_TX	UPC_TA_UART_RX

SIGNAL ALIASES

USB2_UPC_TB_P	RB252 0	USB_UPC_PCH_TB_P
USB2_UPC_TB_N	RB253 0	USB_UPC_PCH_TB_N
USB2_UPC_TA_P	RB256 0	USB_UPC_PCH_TA_P
USB2_UPC_TA_N	RB257 0	USB_UPC_PCH_TA_N
USB_UPC_TB_P	RB250 0	USB_UPC_TB_P (NOSTUFF)
USB_UPC_TB_N	RB251 0	USB_UPC_TB_N (NOSTUFF)
USB_UPC_TA_P	RB354 0	USB_UPC_TA_P (NOSTUFF)
USB_UPC_TA_N	RB255 0	USB_UPC_TA_N (NOSTUFF)

(5% MF 1/20W 0201)

TBT_T_CIO_PWR_EN	TBT_T_CIO_PWR_EN (MAKE_BASE=TRUE)
TBT_T_USB_PWR_EN	TBT_T_USB_PWR_EN (MAKE_BASE=TRUE)
PM_BATLOW_L	PM_BATLOW_L (MAKE_BASE=TRUE)
SMC_PME_S4_DARK_L	SMC_PME_S4_DARK_L (MAKE_BASE=TRUE)
UPC_T_5V_EN	UPC_T_5V_EN (MAKE_BASE=TRUE)
JTAG_ISP_TDO	JTAG_ISP_TDO (MAKE_BASE=TRUE)
SMC_USBC_INT_L (IN)	SMC_USBC_INT_L (OUT) (MAKE_BASE=TRUE)
SSD_DEBUG_I2C_CLK_CONN	SSD_DEBUG_I2C_CLK_CONN (OUT) (MAKE_BASE=TRUE)
SSD_DEBUG_I2C_DAT_CONN	SSD_DEBUG_I2C_DAT_CONN (BI) (MAKE_BASE=TRUE)
TBT_T_CIO_PLUG_EVENT_L	TBT_T_CIO_PLUG_EVENT_L (MAKE_BASE=TRUE)
UPC_TA_FAULT_L (IN)	RB258 0 — XDP_PCH_OBSDATA_C2
UPC_TB_FAULT_L (IN)	RB259 0 — XDP_PCH_OBSDATA_C3
JTAG_TBT_T_TMS	JTAG_TBT_T_TMS (MAKE_BASE=TRUE)
PP3V3_S4	PP3V3_S4 (MAKE_BASE=TRUE)
TP_USBC_TB_RESET_L	TP_USBC_TB_RESET_L (MAKE_BASE=TRUE)
TBT_POC_RESET (IN)	TBT_POC_RESET (MAKE_BASE=TRUE) (OUT)

(5% MF 1/20W 0201)

POWER ALIASES

PP3V3_UPC_TA_LDO	PP3V3_UPC_TA_LDO	MAKE_BASE=TRUE
PP20V_USBC_TA_VBUS	PP20V_USBC_TA_VBUS	MAKE_BASE=TRUE
PP20V_USBC_TB_VBUS	PP20V_USBC_TB_VBUS	MAKE_BASE=TRUE
PP3V3_UPC_TB_LDO	PP3V3_UPC_TB_LDO	MAKE_BASE=TRUE
PP5V_S4_T_USBC	PP5V_S4_T_USBC	MAKE_BASE=TRUE; MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1200 VOLTAGE=5V
PP3V3_TBT_T_S0	PP3V3_TBT_T_S0	MAKE_BASE=TRUE; MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V

NO TEST

NC_UPC_TB_I2C_ADDR

GND ALIASES

GND — MAKE_BASE=TRUE — BOM_COST_GROUP=TBT

PAGE TITLE: USB-C Support

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BRANCH	dvt-fab10
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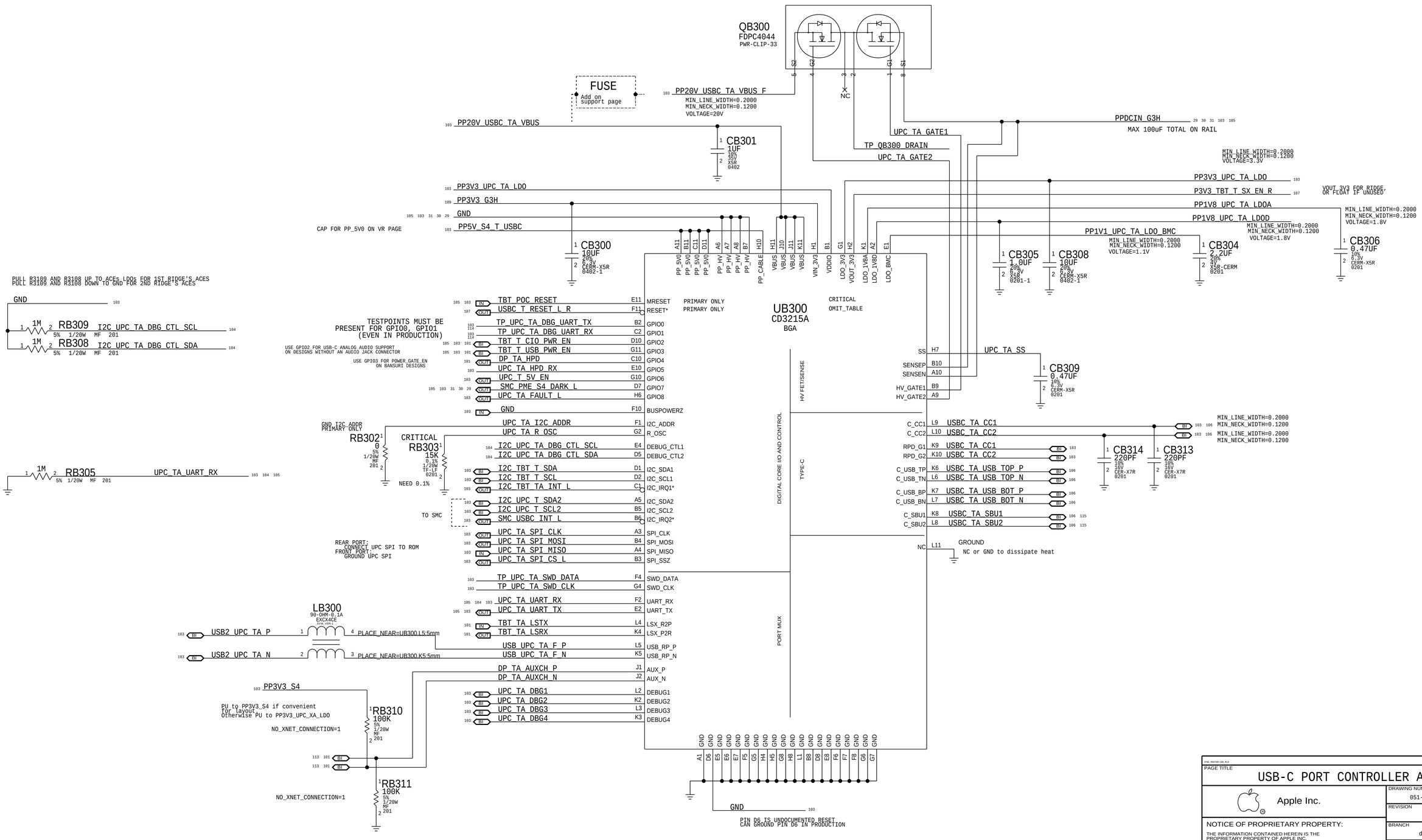
PRIMARY ACE USB-C PORT CONTROLLER (UPC)



BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C PORT CONTROLLER A

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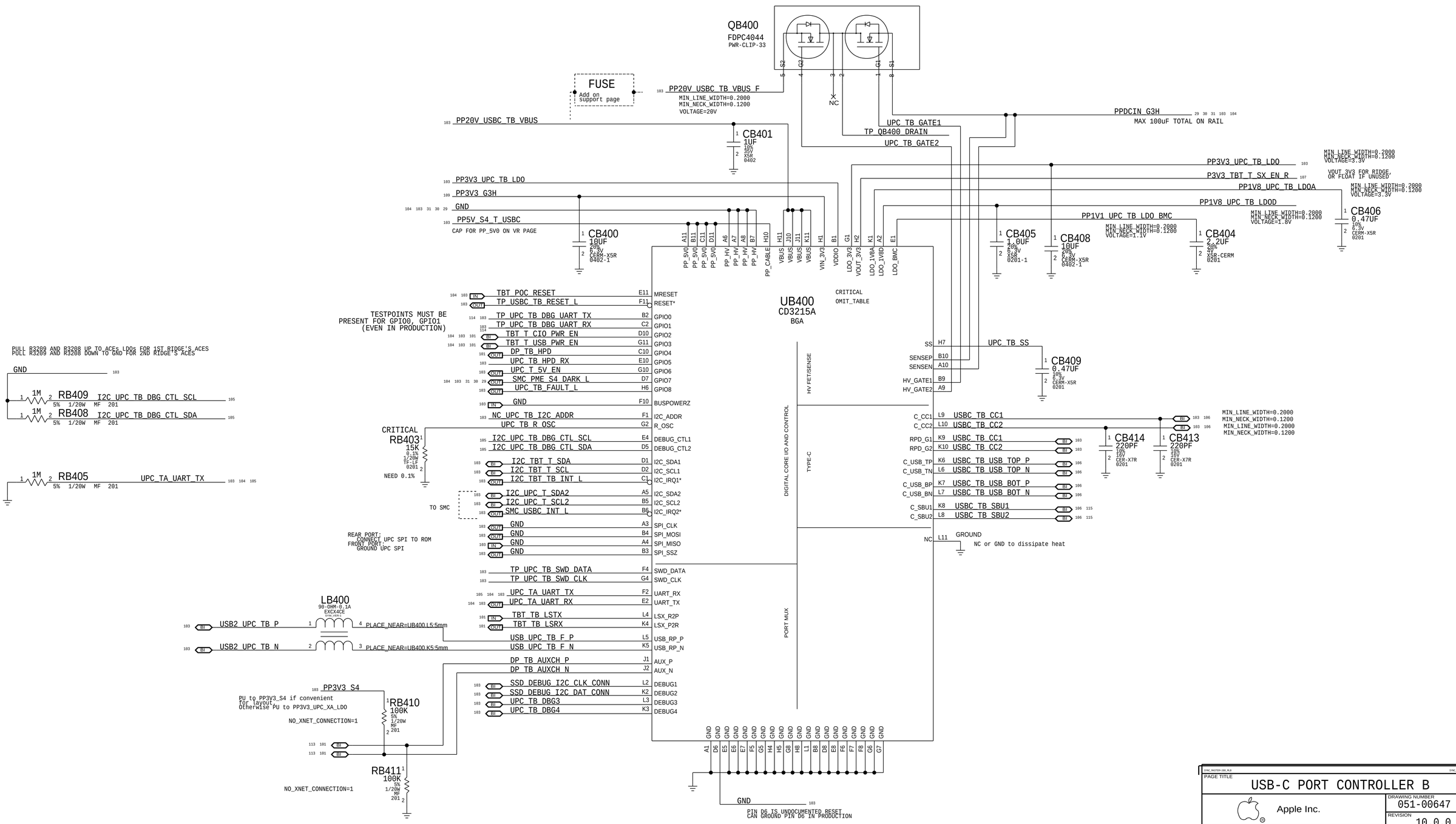
SECONDARY ACE USB-C PORT CONTROLLER (UPC)



BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C PORT CONTROLLER B

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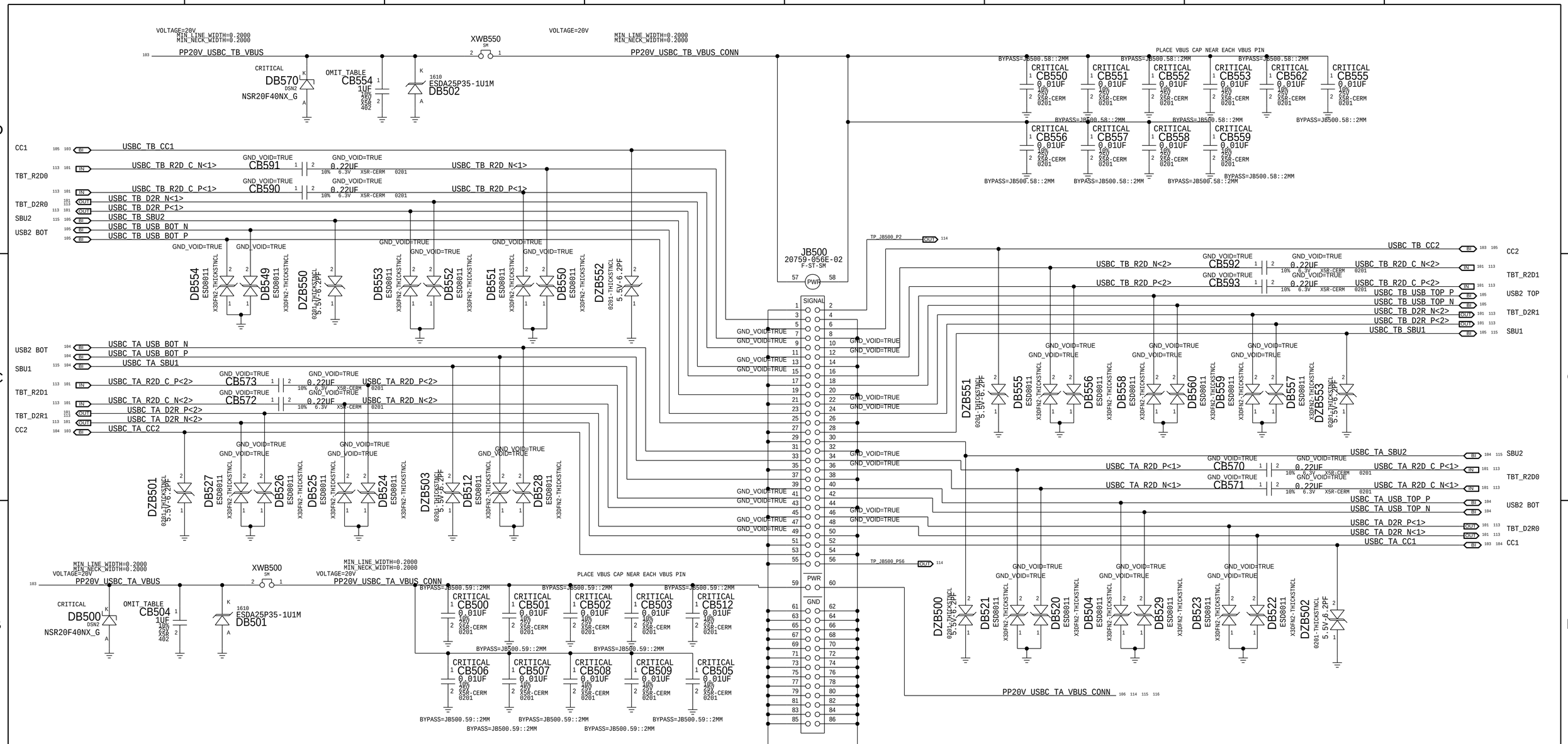

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0683	2	CAP,CER,X5R,1UF,10%,25V,0402	CB504, CB554	CRITICAL	NOSTUFF

LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE
USB-C CONNECTOR A

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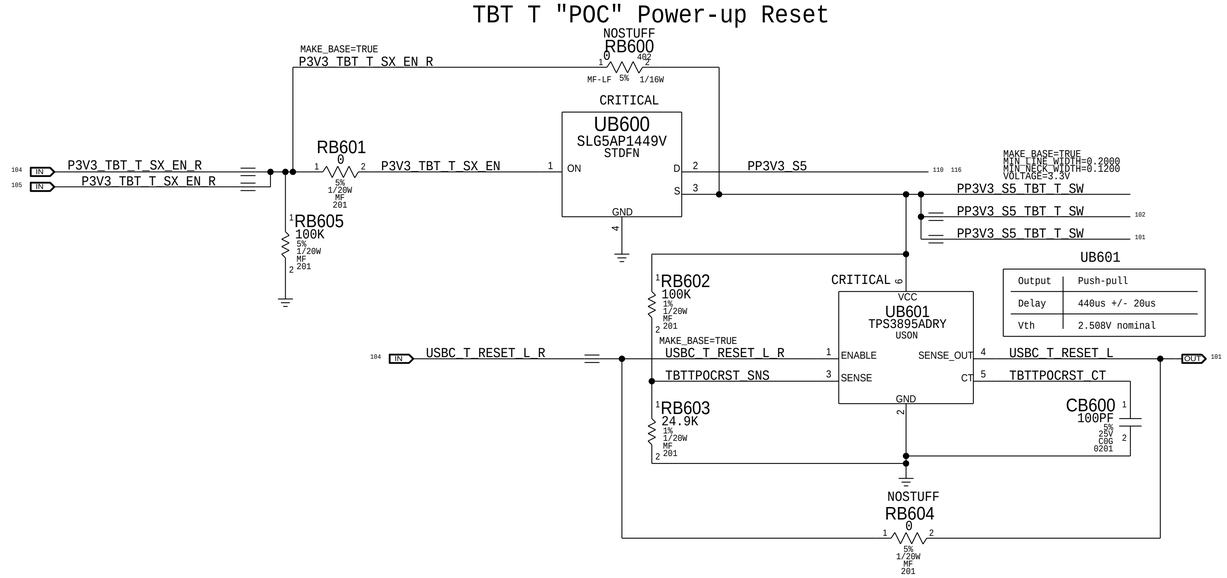
TBT T "POC" Power-up Reset



UB601

Output	Push-pull
Delay	440us +/- 20us
Vth	2.508V nominal

BOM_COST_GROUP=USB-C

DESIGN: j130/dev_mlb_u
LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE
USB-C CONNECTOR B

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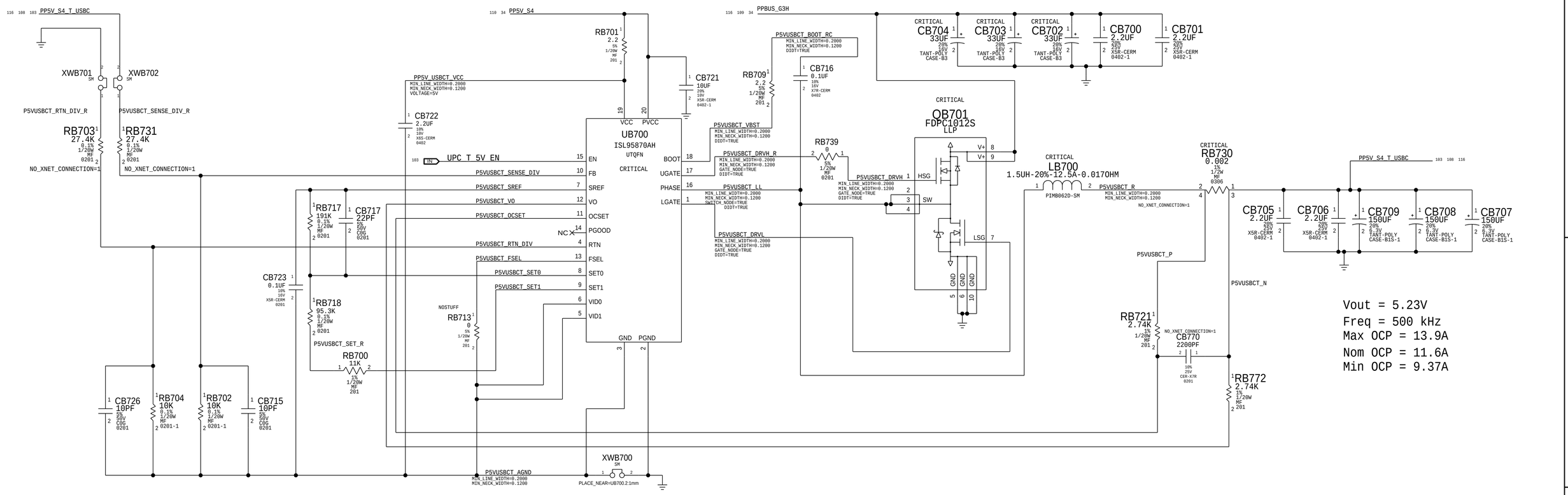

BOM_COST_GROUP=USB-C

PAGE TITLE

TBT 5V REGULATOR

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PBUS Rails

116 64 PPBUS_G3H
PPBUS_G3H
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=13.1V
MAKE_BASE=TRUE
114
PPBUS_G3H 50
PPBUS_G3H 50
PPBUS_G3H 50
PPBUS_G3H 75
PPBUS_G3H 50
PPBUS_G3H 50
PPBUS_G3H 70
PPBUS_G3H 63
PPBUS_G3H 72
PPBUS_G3H 34 108 116
PPBUS_G3H 55
PPBUS_G3H 60 61
PPBUS_G3H 72

50 PPBUS_HS_CPU
PPBUS_HS_CPU
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=13.1V
MAKE_BASE=TRUE
117
PPBUS_HS_CPU 66
PPBUS_HS_CPU 67
PPBUS_HS_CPU 68
PPBUS_HS_CPU 71
PPBUS_HS_CPU 71
PPBUS_HS_CPU 65

55 PPBUS_HS_GPU
PPBUS_HS_GPU
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=13.1V
MAKE_BASE=TRUE
97
PPBUS_HS_GPU 94
PPBUS_HS_GPU 97
PPBUS_HS_GPU 94
PPBUS_HS_GPU 100

50 PPBUS_HS_OTH5V
PPBUS_HS_OTH5V
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=13.1V
MAKE_BASE=TRUE
PPBUS_HS_OTH5V 69 117

117 50 PPBUS_HS_OTH3V3
PPBUS_HS_OTH3V3
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=13.1V
MAKE_BASE=TRUE
PPBUS_HS_OTH3V3 69 117

50 PPBUS_S4_HS_TPAD
PPBUS_S4_HS_TPAD
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=13.1V
MAKE_BASE=TRUE
PPBUS_S4_HS_TPAD 43

3V3 G3H Rails

63 PP3V3_G3H
PP3V3_G3H
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE
114
PP3V3_G3H 57
PP3V3_G3H 46 47 76
PP3V3_G3H 48
PP3V3_G3H 64
PP3V3_G3H 43 48
PP3V3_G3H 49
PP3V3_G3H 48
PP3V3_G3H 47
PP3V3_G3H 20
PP3V3_G3H 49
PP3V3_G3H 30
PP3V3_G3H 31
PP3V3_G3H 29
PP3V3_G3H 104
PP3V3_G3H 105

RTC Rails

70 PP3V0_G3H
PP3V0_G3H
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.0V
MAKE_BASE=TRUE
PP3V0_G3H 12 16 17
PP3V0_G3H 70

IMVP Rails

66 PPVCC_S0_CPU
PPVCC_S0_CPU
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.5V
MAKE_BASE=TRUE
114
PPVCC_S0_CPU 6 8 55
PPVCC_S0_CPU 10

67 PPVCCSA_S0_CPU
PPVCCSA_S0_CPU
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.15V
MAKE_BASE=TRUE
PPVCCSA_S0_CPU 8 53
PPVCCSA_S0_CPU 11

68 PPVCCGT_S0_CPU
PPVCCGT_S0_CPU
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.5V
MAKE_BASE=TRUE
PPVCCGT_S0_CPU 8 55
PPVCCGT_S0_CPU 11 116

CPU VCCIO Rails

117 71 PPVCCIO_S0_CPU
PPVCCIO_S0_CPU
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=0.95V
MAKE_BASE=TRUE
10
PPVCCIO_S0_CPU 5 8

1V2 Rails

117 74 71 PP1V2_S3
PP1V2_S3
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.2V
MAKE_BASE=TRUE
PP1V2_S3 22 23 24 25 116
PP1V2_S3 71 117
PP1V2_S3 21
PP1V2_S3 22 23 24 25
PP1V2_S3 22 23 24 25 116
PP1V2_S3 51
PP1V2_S3 74

51 PP1V2_S3_CPUDDR
PP1V2_S3_CPUDDR
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.2V
MAKE_BASE=TRUE
PP1V2_S3_CPUDDR 8
PP1V2_S3_CPUDDR 10 116

74 PP1V2_S0SW
PP1V2_S0SW
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.2V
MAKE_BASE=TRUE
PP1V2_S0SW 8

0V6 Rails

117 71 PP0V6_S0_DDRVTT
PP0V6_S0_DDRVTT
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=0.6V
MAKE_BASE=TRUE
PP0V6_S0_DDRVTT 26 116
PP0V6_S0_DDRVTT 26 116

21 PP0V6_S3_MEM_VREFDQ_A
PP0V6_S3_MEM_VREFDQ_A
MAKE_BASE=TRUE VOLTAGE=0.6V
22 23
109 21 PP0V6_S3_MEM_VREFCA_A
PP0V6_S3_MEM_VREFCA_A
MAKE_BASE=TRUE VOLTAGE=0.6V
22 23
21 PP0V6_S3_MEM_VREFDQ_B
PP0V6_S3_MEM_VREFDQ_B
MAKE_BASE=TRUE VOLTAGE=0.6V
24 25
109 21 PP0V6_S3_MEM_VREFCA_A
PP0V6_S3_MEM_VREFCA_A
MAKE_BASE=TRUE VOLTAGE=0.6V
24 25

1V8 Rails

117 72 PP1V8_SUS
PP1V8_SUS
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP1V8_SUS 74
PP1V8_SUS 74
PP1V8_SUS 15 16 17

74 PP1V8_S4
PP1V8_S4
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP1V8_S4 38 42
PP1V8_S4 20

74 PP1V8_S3
PP1V8_S3
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP1V8_S3 53
PP1V8_S3 70

53 PP1V8_S3_MEM
PP1V8_S3_MEM
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP1V8_S3_MEM 22 23 24 25 116

74 PP1V8_S0
PP1V8_S0
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V
MAKE_BASE=TRUE
61 114
PP1V8_S0 16 17
PP1V8_S0 58 60 61
PP1V8_S0 37 38 42
PP1V8_S0 73
PP1V8_S0 19
PP1V8_S0 37 42
PP1V8_S0 37

SYNC_MASTER=J08_MLB SYNC_DATE=08/16/2010

PAGE TITLE
Power Aliases - 1

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1V0 Rails

117 72 PP1V0_SUS
PP1V0_SUS
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1V
MAKE_BASE=TRUE
PP1V0_SUS 16 17
PP1V0_SUS 16 17
PP1V0_SUS 16
PP1V0_SUS 16
PP1V0_SUS 16
PP1V0_SUS 16
PP1V0_SUS 17
PP1V0_SUS 17
PP1V0_SUS 18
PP1V0_SUS 74
PP1V0_SUS 12
PP1V0_SUS 17
PP1V0_SUS 20
PP1V0_SUS 16 17

74 PP1V0_S3
PP1V0_S3
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1V
MAKE_BASE=TRUE
PP1V0_S3 6 8 11
PP1V0_S3 65
PP1V0_S3 8 11
PP1V0_S3 74
PP1V0_S3 47

74 PP1V0_S0SW
PP1V0_S0SW
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1V
MAKE_BASE=TRUE
PP1V0_S0SW 6 8 11 18

T208 Rails

51 PP3V3_S5_T139
PP3V3_S5_T139
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S5_T139 42

52 PP3V3_S4_SOC_PMU
PP3V3_S4_SOC_PMU
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S4_SOC_PMU 38 42
PP3V3_S4_SOC_PMU 40 41

52 PP5V_S0_T139
PP5V_S0_T139
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=5V
MAKE_BASE=TRUE
PP5V_S0_T139 42

5V Rails

69 PP5V_S5
PP5V_S5
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=5V
MAKE_BASE=TRUE

117 69 PP5V_S4
PP5V_S4
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=5V
MAKE_BASE=TRUE
PP5V_S4 43
PP5V_S4 51 53
PP5V_S4 74
PP5V_S4 34 108
PP5V_S4 65
PP5V_S4 73

117 74 PP5V_S0
PP5V_S0
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=5V
MAKE_BASE=TRUE
PP5V_S0 38 115
PP5V_S0 52
PP5V_S0 65 66 67
PP5V_S0 117
PP5V_S0 75
PP5V_S0 43 56 117
PP5V_S0 53
PP5V_S0 76
PP5V_S0 68
PP5V_S0 94
PP5V_S0 97
PP5V_S0 100

53 PP5V_S0_KBD
PP5V_S0_KBD
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
MAKE_BASE=TRUE
PP5V_S0_KBD 114
PP5V_S0_KBD 43

3V3 Rails

117 69 PP3V3_S5
PP3V3_S5
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S5 115
PP3V3_S5 12 16 17
PP3V3_S5 74
PP3V3_S5 74
PP3V3_S5 74
PP3V3_S5 70
PP3V3_S5 117
PP3V3_S5 20
PP3V3_S5 74
PP3V3_S5 72
PP3V3_S5 19
PP3V3_S5 74
PP3V3_S5 74
PP3V3_S5 74
PP3V3_S5 74
PP3V3_S5 76
PP3V3_S5 51
PP3V3_S5 87
PP3V3_S5 100
PP3V3_S5 89
PP3V3_S5 74
PP3V3_S5 33 116
PP3V3_S5 107 116
PP3V3_S5 114

74 PP3V3_SUS
PP3V3_SUS
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_SUS 57
PP3V3_SUS 12 14 16 17
PP3V3_SUS 16 17
PP3V3_SUS 16 17
PP3V3_SUS 12 15 16 17
PP3V3_SUS 13 16 17
PP3V3_SUS 16 17
PP3V3_SUS 15 16 17
PP3V3_SUS 70
PP3V3_SUS 18 73
PP3V3_SUS 74
PP3V3_SUS 70
PP3V3_SUS 43
PP3V3_SUS 114

117 74 PP3V3_S4
PP3V3_S4
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S4 29 103 114
PP3V3_S4 51
PP3V3_S4 51
PP3V3_S4 52
PP3V3_S4 43
PP3V3_S4 49
PP3V3_S4 12
PP3V3_S4 52
PP3V3_S4 35
PP3V3_S4 47 48
PP3V3_S4 52
PP3V3_S4 89

52 PP3V3_S4_T151
PP3V3_S4_T151
MAKE_BASE=TRUE
PP3V3_S4_T151 45

51 PP3V3_S4_BT
PP3V3_S4_BT
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S4_BT 35

51 PP3V3_S4_WLAN
PP3V3_S4_WLAN
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1800
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S4_WLAN 36

52 PP3V3_S4_TPAD
PP3V3_S4_TPAD
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S4_TPAD 43

74 PP3V3_S4SW_SNS
PP3V3_S4SW_SNS
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S4SW_SNS 50
PP3V3_S4SW_SNS 50 51 52 53 55

91 74 PP3V3_S0
PP3V3_S0
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S0 114
PP3V3_S0 53
PP3V3_S0 56
PP3V3_S0 54
PP3V3_S0 12 14 20 73
PP3V3_S0 49
PP3V3_S0 49
PP3V3_S0 49
PP3V3_S0 49
PP3V3_S0 52
PP3V3_S0 51
PP3V3_S0 51
PP3V3_S0 20
PP3V3_S0 54
PP3V3_S0 47
PP3V3_S0 76
PP3V3_S0 47
PP3V3_S0 59
PP3V3_S0 12 13 15
PP3V3_S0 52
PP3V3_S0 16 17
PP3V3_S0 100
PP3V3_S0 49 89 98
PP3V3_S0 89
PP3V3_S0 100
PP3V3_S0 43

91 74 PP3V3_S0_LEFT
PP3V3_S0_LEFT
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S0_LEFT 56
PP3V3_S0_LEFT 54
PP3V3_S0_LEFT 52
PP3V3_S0_LEFT 50
PP3V3_S0_LEFT 52
PP3V3_S0_LEFT 38 42
PP3V3_S0_LEFT 42
PP3V3_S0_LEFT 37
PP3V3_S0_LEFT 70
PP3V3_S0_LEFT 54

52 PP3V3_TBT_X_S0
PP3V3_TBT_X_S0 28 29 116

52 PP3V3_TBT_T_S0
PP3V3_TBT_T_S0 102 103 116

GPU Rails

97 PPVCORE_S0_GPU
PPVCORE_S0_GPU
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V
MAKE_BASE=TRUE
PPVCORE_S0_GPU 55 90 92

94 PPVDDCI_S0_GPU
PPVDDCI_S0_GPU
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V
MAKE_BASE=TRUE
PPVDDCI_S0_GPU 92
PPVDDCI_S0_GPU 99
PPVDDCI_S0_GPU 55 92

116 94 PP1V5R1V35_S0_GPU_MEM
PP1V5R1V35_S0_GPU_MEM
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.5V
MAKE_BASE=TRUE
PP1V5R1V35_S0_GPU_MEM 92
PP1V5R1V35_S0_GPU_MEM 95 96
PP1V5R1V35_S0_GPU_MEM 55

55 PP1V5R1V35_S0_GPU_IC
PP1V5R1V35_S0_GPU_IC
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.5V
MAKE_BASE=TRUE
PP1V5R1V35_S0_GPU_IC 93
PP1V5R1V35_S0_GPU_IC 92

116 100 PP1V8_GPU
PP1V8_GPU
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP1V8_GPU 55

116 55 PP1V8_S0_GPU
PP1V8_S0_GPU
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP1V8_S0_GPU 91 99
PP1V8_S0_GPU 92
PP1V8_S0_GPU 99
PP1V8_S0_GPU 98
PP1V8_S0_GPU 97
PP1V8_S0_GPU 98

100 PP3V3_S0_GPU
PP3V3_S0_GPU
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S0_GPU 93 99
PP3V3_S0_GPU 92
PP3V3_S0_GPU 91
PP3V3_S0_GPU 98
PP3V3_S0_GPU 98
PP3V3_S0_GPU 99
PP3V3_S0_GPU 98
PP3V3_S0_GPU 90 94 97 99
PP3V3_S0_GPU 98

Digital Ground

GND
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.1270

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Power Aliases - 2

Apple Inc.

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SIGNAL ALIAS

NC ALIASES 2

NC_CLKOUT_PCIE_1_N	MAKE_BASE=TRUE	NC_CLKOUT_PCIE_1_N	MAKE_BASE=TRUE
NC_CLKOUT_PCIE_1_P	MAKE_BASE=TRUE	NC_CLKOUT_PCIE_1_P	MAKE_BASE=TRUE
NC_CLKOUT_PCIE_2_N	MAKE_BASE=TRUE	NC_CLKOUT_PCIE_2_N	MAKE_BASE=TRUE
NC_CLKOUT_PCIE_2_P	MAKE_BASE=TRUE	NC_CLKOUT_PCIE_2_P	MAKE_BASE=TRUE
NC_CLKOUT_PCIE_6_N	MAKE_BASE=TRUE	NC_CLKOUT_PCIE_6_N	MAKE_BASE=TRUE
NC_CLKOUT_PCIE_6_P	MAKE_BASE=TRUE	NC_CLKOUT_PCIE_6_P	MAKE_BASE=TRUE
NC_CLKOUT_PCIE_8_N	MAKE_BASE=TRUE	NC_CLKOUT_PCIE_8_N	MAKE_BASE=TRUE
NC_CLKOUT_PCIE_8_P	MAKE_BASE=TRUE	NC_CLKOUT_PCIE_8_P	MAKE_BASE=TRUE
NC_CLKOUT_PCIE_9_N	MAKE_BASE=TRUE	NC_CLKOUT_PCIE_9_N	MAKE_BASE=TRUE
NC_CLKOUT_PCIE_9_P	MAKE_BASE=TRUE	NC_CLKOUT_PCIE_9_P	MAKE_BASE=TRUE
NC_CLKOUT_PCIE_10_N	MAKE_BASE=TRUE	NC_CLKOUT_PCIE_10_N	MAKE_BASE=TRUE
NC_CLKOUT_PCIE_10_P	MAKE_BASE=TRUE	NC_CLKOUT_PCIE_10_P	MAKE_BASE=TRUE
NC_CLKOUT_PCIE_11_N	MAKE_BASE=TRUE	NC_CLKOUT_PCIE_11_N	MAKE_BASE=TRUE
NC_CLKOUT_PCIE_11_P	MAKE_BASE=TRUE	NC_CLKOUT_PCIE_11_P	MAKE_BASE=TRUE
NC_CLKOUT_PCIE_12_N	MAKE_BASE=TRUE	NC_CLKOUT_PCIE_12_N	MAKE_BASE=TRUE
NC_CLKOUT_PCIE_12_P	MAKE_BASE=TRUE	NC_CLKOUT_PCIE_12_P	MAKE_BASE=TRUE
NC_CLKOUT_PCIE_14_N	MAKE_BASE=TRUE	NC_CLKOUT_PCIE_14_N	MAKE_BASE=TRUE
NC_CLKOUT_PCIE_14_P	MAKE_BASE=TRUE	NC_CLKOUT_PCIE_14_P	MAKE_BASE=TRUE
NC_CLKOUT_PCIE_15_N	MAKE_BASE=TRUE	NC_CLKOUT_PCIE_15_N	MAKE_BASE=TRUE
NC_CLKOUT_PCIE_15_P	MAKE_BASE=TRUE	NC_CLKOUT_PCIE_15_P	MAKE_BASE=TRUE

NC_TP_PCH_GPP_G1	MAKE_BASE=TRUE	NC_TP_PCH_GPP_G1	MAKE_BASE=TRUE
NC_TP_PCH_GPP_G2	MAKE_BASE=TRUE	NC_TP_PCH_GPP_G2	MAKE_BASE=TRUE
NC_TP_PCH_GPP_G3	MAKE_BASE=TRUE	NC_TP_PCH_GPP_G3	MAKE_BASE=TRUE
NC_TP_PCH_GPP_G4	MAKE_BASE=TRUE	NC_TP_PCH_GPP_G4	MAKE_BASE=TRUE
NC_TP_PCH_GPP_G5	MAKE_BASE=TRUE	NC_TP_PCH_GPP_G5	MAKE_BASE=TRUE
NC_TP_PCH_GPP_G6	MAKE_BASE=TRUE	NC_TP_PCH_GPP_G6	MAKE_BASE=TRUE
NC_TP_PCH_GPP_G7	MAKE_BASE=TRUE	NC_TP_PCH_GPP_G7	MAKE_BASE=TRUE
NC_TP_PCH_GPP_G8	MAKE_BASE=TRUE	NC_TP_PCH_GPP_G8	MAKE_BASE=TRUE

NC_PCH_GPP_F15	MAKE_BASE=TRUE	NC_PCH_GPP_F15	MAKE_BASE=TRUE
NC_PCH_GPP_F16	MAKE_BASE=TRUE	NC_PCH_GPP_F16	MAKE_BASE=TRUE
NC_PCH_GPP_F17	MAKE_BASE=TRUE	NC_PCH_GPP_F17	MAKE_BASE=TRUE
NC_PCH_GPP_F18	MAKE_BASE=TRUE	NC_PCH_GPP_F18	MAKE_BASE=TRUE

GPU PEG Lanes

IN	PEG_GPU_D2R_P<7..0>	MAKE_BASE=TRUE	=PEG_D2R_P<7..0>	OUT
IN	PEG_GPU_D2R_N<7..0>	MAKE_BASE=TRUE	=PEG_D2R_N<7..0>	OUT
OUT	PEG_GPU_R2D_C_P<7..0>	MAKE_BASE=TRUE	=PEG_R2D_C_P<7..0>	IN
OUT	PEG_GPU_R2D_C_N<7..0>	MAKE_BASE=TRUE	=PEG_R2D_C_N<7..0>	IN

Thunderbolt Signals Through PEG

IN	PCIE_TBT_X_D2R_P<3..0>	MAKE_BASE=TRUE	=PEG_D2R_P<11..8>	OUT
IN	PCIE_TBT_X_D2R_N<3..0>	MAKE_BASE=TRUE	=PEG_D2R_N<11..8>	OUT
OUT	PCIE_TBT_X_R2D_C_P<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_P<11..8>	IN
OUT	PCIE_TBT_X_R2D_C_N<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_N<11..8>	IN
IN	PCIE_TBT_T_D2R_P<3..0>	MAKE_BASE=TRUE	=PEG_D2R_P<15..12>	OUT
IN	PCIE_TBT_T_D2R_N<3..0>	MAKE_BASE=TRUE	=PEG_D2R_N<15..12>	OUT
OUT	PCIE_TBT_T_R2D_C_P<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_P<15..12>	IN
OUT	PCIE_TBT_T_R2D_C_N<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_N<15..12>	IN

GPU ALIAS

EG_CLKREQ_OUT_L	MAKE_BASE=TRUE	EG_CLKREQ_OUT_L	MAKE_BASE=TRUE
EG_PEG_CLK100M_N	MAKE_BASE=TRUE	EG_PEG_CLK100M_N	MAKE_BASE=TRUE
EG_PEG_CLK100M_P	MAKE_BASE=TRUE	EG_PEG_CLK100M_P	MAKE_BASE=TRUE
EG_RESET_L		EG_RESET_L	

CPU Display Aliases

eDP conn		DPMUX	
EDP_INT_ML_P<3..0>	MAKE_BASE=TRUE	EDP_INT_ML_P<3..0>	
EDP_INT_ML_N<3..0>	MAKE_BASE=TRUE	EDP_INT_ML_N<3..0>	
EDP_AUXCH_C_P	MAKE_BASE=TRUE	EDP_AUXCH_C_P	
EDP_AUXCH_C_N	MAKE_BASE=TRUE	EDP_AUXCH_C_N	
NC_DDI1_ML_C_P<3..0>	MAKE_BASE=TRUE NO_TEST=1	NC_DDI1_ML_C_P<3..0>	
NC_DDI1_ML_C_N<3..0>	MAKE_BASE=TRUE NO_TEST=1	NC_DDI1_ML_C_N<3..0>	
NC_DDI1_AUXCH_C_P	MAKE_BASE=TRUE	NC_DDI1_AUXCH_C_P	
NC_DDI1_AUXCH_C_N	MAKE_BASE=TRUE	NC_DDI1_AUXCH_C_N	
NC_DDI2_ML_C_P<3..0>	MAKE_BASE=TRUE NO_TEST=1	NC_DDI2_ML_C_P<3..0>	
NC_DDI2_ML_C_N<3..0>	MAKE_BASE=TRUE NO_TEST=1	NC_DDI2_ML_C_N<3..0>	
NC_DDI2_AUXCH_C_P	MAKE_BASE=TRUE	NC_DDI2_AUXCH_C_P	
NC_DDI2_AUXCH_C_N	MAKE_BASE=TRUE	NC_DDI2_AUXCH_C_N	
NC_DDI3_ML_P<3..0>	MAKE_BASE=TRUE NO_TEST=1	NC_DDI3_ML_P<3..0>	
NC_DDI3_ML_N<3..0>	MAKE_BASE=TRUE NO_TEST=1	NC_DDI3_ML_N<3..0>	
NC_DDI3_AUXCH_P	MAKE_BASE=TRUE	NC_DDI3_AUXCH_P	
NC_DDI3_AUXCH_N	MAKE_BASE=TRUE	NC_DDI3_AUXCH_N	
DPMUX_UC_RX		DPMUX_UC_RX	
DPMUX_UC_TX	MAKE_BASE=TRUE	DPMUX_UC_TX	
NC_EDP_IG_BKLT_PWM	MAKE_BASE=TRUE	NC_EDP_IG_BKLT_PWM	MAKE_BASE=TRUE

EPD PANEL

I2C_BKLT_SCL	MAKE_BASE TRUE	I2C_BKLT_SCL	
I2C_BKLT_SDA	MAKE_BASE TRUE	I2C_BKLT_SDA	

UNUSED SIGNALS

NC_PCH_SLP_WLAN_L	MAKE_BASE=TRUE	NC_PCH_SLP_WLAN_L
NC_SPI_CS1_L	MAKE_BASE=TRUE	NC_SPI_CS1_L
NC_SPI_CS2_L	MAKE_BASE=TRUE	NC_SPI_CS2_L

SYNC_MASTER=X363_SANXOC SYNC_DATE=01/13/2015

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Signal Aliases

Apple Inc.

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REVISION	10.0.0
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Memory Bit/Byte Swizzle

LPDDR3 COMMAND/ADDRESS

BDW-H LPDDR3 NET	BIT SWIZZLE
MAKE_BASE=TRUE	
MEM_A_DQ<0>	MEM_A_DQ<0>
MEM_A_DQ<1>	MEM_A_DQ<1>
MEM_A_DQ<2>	MEM_A_DQ<2>
MEM_A_DQ<3>	MEM_A_DQ<3>
MEM_A_DQ<4>	MEM_A_DQ<4>
MEM_A_DQ<5>	MEM_A_DQ<5>
MEM_A_DQ<6>	MEM_A_DQ<6>
MEM_A_DQ<7>	MEM_A_DQ<7>
MEM_A_DQ<8>	MEM_A_DQ<8>
MEM_A_DQ<9>	MEM_A_DQ<9>
MEM_A_DQ<10>	MEM_A_DQ<10>
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MEM_A_DQ<13>	MEM_A_DQ<13>
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BDW-H LPDDR3 NET	BIT SWIZZLE
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MEM_B_DQ<2>	MEM_B_DQ<2>
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MEM_B_DQ<61>	MEM_B_DQ<61>
MEM_B_DQ<62>	MEM_B_DQ<62>
MEM_B_DQ<63>	MEM_B_DQ<63>

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TRUE	MEM_A_DQS_N<0>	MEM_A_DQS_N<0>
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TRUE	MEM_A_DQS_N<1>	MEM_A_DQS_N<1>
TRUE	MEM_A_DQS_P<2>	MEM_A_DQS_P<2>
TRUE	MEM_A_DQS_N<2>	MEM_A_DQS_N<2>
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TRUE	MEM_A_DQS_N<3>	MEM_A_DQS_N<3>
TRUE	MEM_A_DQS_P<4>	MEM_A_DQS_P<4>
TRUE	MEM_A_DQS_N<4>	MEM_A_DQS_N<4>
TRUE	MEM_A_DQS_P<5>	MEM_A_DQS_P<5>
TRUE	MEM_A_DQS_N<5>	MEM_A_DQS_N<5>
TRUE	MEM_A_DQS_P<6>	MEM_A_DQS_P<6>
TRUE	MEM_A_DQS_N<6>	MEM_A_DQS_N<6>
TRUE	MEM_A_DQS_P<7>	MEM_A_DQS_P<7>
TRUE	MEM_A_DQS_N<7>	MEM_A_DQS_N<7>

MAKE_BASE		
TRUE	MEM_B_DQS_P<0>	MEM_B_DQS_P<0>
TRUE	MEM_B_DQS_N<0>	MEM_B_DQS_N<0>
TRUE	MEM_B_DQS_P<1>	MEM_B_DQS_P<1>
TRUE	MEM_B_DQS_N<1>	MEM_B_DQS_N<1>
TRUE	MEM_B_DQS_P<2>	MEM_B_DQS_P<2>
TRUE	MEM_B_DQS_N<2>	MEM_B_DQS_N<2>
TRUE	MEM_B_DQS_P<3>	MEM_B_DQS_P<3>
TRUE	MEM_B_DQS_N<3>	MEM_B_DQS_N<3>
TRUE	MEM_B_DQS_P<4>	MEM_B_DQS_P<4>
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TRUE	MEM_B_DQS_N<5>	MEM_B_DQS_N<5>
TRUE	MEM_B_DQS_P<6>	MEM_B_DQS_P<6>
TRUE	MEM_B_DQS_N<6>	MEM_B_DQS_N<6>
TRUE	MEM_B_DQS_P<7>	MEM_B_DQS_P<7>
TRUE	MEM_B_DQS_N<7>	MEM_B_DQS_N<7>

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE: Memory Bit/Byte Swizzle

Apple Inc.

DRAWING NUMBER: 051-00647 SIZE: D

REVISION: 10.0.0

BRANCH: dvt-fab10

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High Speed NO_TEST

DMI

13 5	IN	DMI_S2N_P<3..0>	NO_TEST=1
13 5	IN	DMI_S2N_N<3..0>	NO_TEST=1
13 5	IN	DMI_N2S_P<3..0>	NO_TEST=1
13 5	IN	DMI_N2S_N<3..0>	NO_TEST=1

DP - CPU/ACE

99 27	IN	DP_X_SNK0_ML_C_N<3..0>	NO_TEST=1
99 27	IN	DP_X_SNK0_ML_C_P<3..0>	NO_TEST=1
27	IN	DP_X_SNK0_ML_N<3..0>	NO_TEST=1
27	IN	DP_X_SNK0_ML_P<3..0>	NO_TEST=1
99 27	IN	DP_X_SNK1_ML_C_N<3..0>	NO_TEST=1
99 27	IN	DP_X_SNK1_ML_C_P<3..0>	NO_TEST=1
27	IN	DP_X_SNK1_ML_N<3..0>	NO_TEST=1
27	IN	DP_X_SNK1_ML_P<3..0>	NO_TEST=1
101 99	IN	DP_T_SNK0_ML_C_N<3..0>	NO_TEST=1
101 99	IN	DP_T_SNK0_ML_C_P<3..0>	NO_TEST=1
101	IN	DP_T_SNK0_ML_N<3..0>	NO_TEST=1
101	IN	DP_T_SNK0_ML_P<3..0>	NO_TEST=1
101 99	IN	DP_T_SNK1_ML_C_N<3..0>	NO_TEST=1
101 99	IN	DP_T_SNK1_ML_C_P<3..0>	NO_TEST=1
101	IN	DP_T_SNK1_ML_N<3..0>	NO_TEST=1
101	IN	DP_T_SNK1_ML_P<3..0>	NO_TEST=1
99 27	IN	DP_X_SNK0_AUXCH_C_P	NO_TEST=1
99 27	IN	DP_X_SNK0_AUXCH_C_N	NO_TEST=1
101 99	IN	DP_T_SNK0_AUXCH_C_P	NO_TEST=1
101 99	IN	DP_T_SNK0_AUXCH_C_N	NO_TEST=1
27	IN	DP_X_SNK0_AUXCH_P	NO_TEST=1
27	IN	DP_X_SNK0_AUXCH_N	NO_TEST=1
101	IN	DP_T_SNK0_AUXCH_P	NO_TEST=1
101	IN	DP_T_SNK0_AUXCH_N	NO_TEST=1
99 27	IN	DP_X_SNK1_AUXCH_C_P	NO_TEST=1
99 27	IN	DP_X_SNK1_AUXCH_C_N	NO_TEST=1
101 99	IN	DP_T_SNK1_AUXCH_C_P	NO_TEST=1
101 99	IN	DP_T_SNK1_AUXCH_C_N	NO_TEST=1
27	IN	DP_X_SNK1_AUXCH_P	NO_TEST=1
27	IN	DP_X_SNK1_AUXCH_N	NO_TEST=1
101	IN	DP_T_SNK1_AUXCH_P	NO_TEST=1
101	IN	DP_T_SNK1_AUXCH_N	NO_TEST=1

CPU/EDP

111 76	IN	EDP_AUXCH_C_N	
111 76	IN	EDP_AUXCH_C_P	

PCH/AR

35 14	IN	PCIE_AP_D2R_P	NO_TEST=1
35 14	IN	PCIE_AP_D2R_N	NO_TEST=1
35	IN	PCIE_AP_R2D_P	NO_TEST=1
35	IN	PCIE_AP_R2D_N	NO_TEST=1
35 14	IN	PCIE_AP_R2D_C_P	NO_TEST=1
35 14	IN	PCIE_AP_R2D_C_N	NO_TEST=1

PCH/SSD

87 77 14	IN	PCIE_SSD_D2R_N<3..0>	NO_TEST=1
87 77 14	IN	PCIE_SSD_D2R_P<3..0>	NO_TEST=1
113 77	IN	PCIE_SSD_R2D_N<3..0>	NO_TEST=1
113 77	IN	PCIE_SSD_R2D_P<3..0>	NO_TEST=1
77	IN	PCIE_SSD_D2R_C_N<3..0>	NO_TEST=1
113 87 77 14	IN	PCIE_SSD_R2D_C_N<3..0>	NO_TEST=1
14	IN	PCIE_SSD_D2R_N<0>	NO_TEST=1
14	IN	PCIE_SSD_D2R_P<0>	NO_TEST=1
77	IN	PCIE_SSD_D2R_C_P<3..0>	NO_TEST=1
113 87 77 14	IN	PCIE_SSD_R2D_C_N<3..0>	NO_TEST=1
87 77	IN	PCIE_SSD_D2R_LB_P<0>	
87 77	IN	PCIE_SSD_R2D_LB_N<0>	
14	IN	PCIE_SSD_D2R_P<3>	NO_TEST=1
87 77	IN	PCIE_SSD_D2R_LB_N<0>	
14	IN	PCIE_SSD_D2R_N<3>	NO_TEST=1
87 77	IN	PCIE_SSD_R2D_LB_P<0>	

USB-C X

32 27	IN	USBC_XB_D2R_N<2..1>	NO_TEST=1
32 27	IN	USBC_XB_D2R_P<2..1>	NO_TEST=1
32 27	IN	USBC_XA_D2R_P<2..1>	NO_TEST=1
32 27	IN	USBC_XB_R2D_C_P<2..1>	NO_TEST=1
30 27	IN	DP_XA_AUXCH_P	NO_TEST=1
32 27	IN	USBC_XA_D2R_N<2..1>	NO_TEST=1
32 27	IN	USBC_XB_R2D_C_N<2..1>	NO_TEST=1
32 27	IN	USBC_XA_R2D_C_P<2..1>	NO_TEST=1
31 27	IN	DP_XB_AUXCH_P	NO_TEST=1
32 27	IN	USBC_XA_R2D_C_N<2..1>	NO_TEST=1
31 27	IN	DP_XB_AUXCH_N	NO_TEST=1
30 27	IN	DP_XA_AUXCH_N	NO_TEST=1
27	IN	DP_XA_AUXCH_C_N	NO_TEST=1
27	IN	DP_XA_AUXCH_C_P	NO_TEST=1
27	IN	DP_XB_AUXCH_C_P	NO_TEST=1
27	IN	DP_XB_AUXCH_C_N	NO_TEST=1

PEG

111 91	IN	PEG_GPU_D2R_N<7..0>	NO_TEST=1
111 91	IN	PEG_GPU_D2R_P<7..0>	NO_TEST=1
111 91	IN	PEG_GPU_R2D_C_N<7..0>	NO_TEST=1
111 91	IN	PEG_GPU_R2D_C_P<7..0>	NO_TEST=1
111 29	IN	PCIE_TBT_X_D2R_P<3..0>	NO_TEST=1
111 29	IN	PCIE_TBT_X_D2R_N<3..0>	NO_TEST=1
111 29	IN	PCIE_TBT_X_R2D_C_P<3..0>	NO_TEST=1
111 29	IN	PCIE_TBT_X_R2D_C_N<3..0>	NO_TEST=1
111 103	IN	PCIE_TBT_T_D2R_P<3..0>	NO_TEST=1
111 103	IN	PCIE_TBT_T_D2R_N<3..0>	NO_TEST=1
103 101	IN	PCIE_TBT_T_D2R_C_P<3..0>	NO_TEST=1
103 101	IN	PCIE_TBT_T_D2R_C_N<3..0>	NO_TEST=1
29 27	IN	PCIE_TBT_X_D2R_C_P<3..0>	NO_TEST=1
29 27	IN	PCIE_TBT_X_D2R_C_N<3..0>	NO_TEST=1
29 27	IN	PCIE_TBT_X_R2D_P<3..0>	NO_TEST=1
29 27	IN	PCIE_TBT_X_R2D_N<3..0>	NO_TEST=1
103 101	IN	PCIE_TBT_T_R2D_P<3..0>	NO_TEST=1
103 101	IN	PCIE_TBT_T_R2D_N<3..0>	NO_TEST=1
111 103	IN	PCIE_TBT_T_R2D_C_P<3..0>	NO_TEST=1
111 103	IN	PCIE_TBT_T_R2D_C_N<3..0>	NO_TEST=1
91	IN	PEG_GPU_D2R_C_N<7..0>	NO_TEST=1
91	IN	PEG_GPU_D2R_C_P<7..0>	NO_TEST=1
91	IN	PEG_GPU_R2D_N<7..0>	NO_TEST=1
91	IN	PEG_GPU_R2D_P<7..0>	NO_TEST=1

PCH/DFR

38 14	IN	USB_CAMERA_DFR_N	
38 14	IN	USB_CAMERA_DFR_P	

BAFFIN FRAME BUFFER

95 93	IN	FB_A1_CS_L	NO_TEST=1
95 93	IN	FB_A0_CKE_L	NO_TEST=1
95 93	IN	FB_A1_CKE_L	NO_TEST=1
95 93	IN	FB_A0_WE_L	NO_TEST=1
95 93	IN	FB_A1_WE_L	NO_TEST=1
96 93	IN	FB_B1_CS_L	NO_TEST=1
96 93	IN	FB_B0_CKE_L	NO_TEST=1
96 93	IN	FB_B1_CKE_L	NO_TEST=1
113 96 93	IN	FB_B0_WE_L	NO_TEST=1
113 96 93	IN	FB_B0_WE_L	NO_TEST=1
96 93	IN	FB_B0_CLK_P	NO_TEST=1
96 93	IN	FB_B1_CLK_N	NO_TEST=1
96 93	IN	FB_B1_CLK_P	NO_TEST=1
96 93	IN	FB_B0_RAS_L	NO_TEST=1
96 93	IN	FB_B1_RAS_L	NO_TEST=1
96 93	IN	FB_B0_CAS_L	NO_TEST=1
96 93	IN	FB_B1_CAS_L	NO_TEST=1
96 93	IN	FB_B0_CS_L	NO_TEST=1
95 93	IN	FB_A0_DQ<31..0>	NO_TEST=1
95 93	IN	FB_A1_DQ<31..0>	NO_TEST=1
95 93	IN	FB_A0_A<8..0>	NO_TEST=1
95 93	IN	FB_A1_A<8..0>	NO_TEST=1
95 93	IN	FB_A0_WCLK_N<1..0>	NO_TEST=1
95 93	IN	FB_A0_WCLK_P<1..0>	NO_TEST=1
95 93	IN	FB_A1_WCLK_N<1..0>	NO_TEST=1
95 93	IN	FB_A1_WCLK_P<1..0>	NO_TEST=1
95 93	IN	FB_A0_EDC<3..0>	NO_TEST=1
95 93	IN	FB_A1_EDC<3..0>	NO_TEST=1
95 93	IN	FB_A0_DBI_L<3..0>	NO_TEST=1
95 93	IN	FB_A1_DBI_L<3..0>	NO_TEST=1
95 93	IN	FB_A0_ABI_L	NO_TEST=1
95 93	IN	FB_A1_ABI_L	NO_TEST=1
95 93	IN	FB_A0_CLK_N	NO_TEST=1
95 93	IN	FB_A0_CLK_P	NO_TEST=1
95 93	IN	FB_A1_CLK_N	NO_TEST=1
95 93	IN	FB_A1_CLK_P	NO_TEST=1
95 93	IN	FB_A0_RAS_L	NO_TEST=1
95 93	IN	FB_A1_RAS_L	NO_TEST=1
95 93	IN	FB_A0_CAS_L	NO_TEST=1
95 93	IN	FB_A1_CAS_L	NO_TEST=1
95 93	IN	FB_A0_CS_L	NO_TEST=1
96 93	IN	FB_B0_CLK_N	NO_TEST=1
96 93	IN	FB_B0_DQ<31..0>	NO_TEST=1
96 93	IN	FB_B1_DQ<31..0>	NO_TEST=1
96 93	IN	FB_B0_A<8..0>	NO_TEST=1
96 93	IN	FB_B1_A<8..0>	NO_TEST=1
96 93	IN	FB_B0_WCLK_N<1..0>	NO_TEST=1
96 93	IN	FB_B0_WCLK_P<1..0>	NO_TEST=1
96 93	IN	FB_B1_WCLK_N<1..0>	NO_TEST=1
96 93	IN	FB_B1_WCLK_P<1..0>	NO_TEST=1
96 93	IN	FB_B0_EDC<3..0>	NO_TEST=1
96 93	IN	FB_B1_EDC<3..0>	NO_TEST=1
96 93	IN	FB_B0_DBI_L<3..0>	NO_TEST=1
96 93	IN	FB_B1_DBI_L<3..0>	NO_TEST=1
96 93	IN	FB_B0_ABI_L	NO_TEST=1
96 93	IN	FB_B1_ABI_L	NO_TEST=1

CPU/PCH CLK

12 6	IN	CPU_CLK24M_NSSC_CLK_N	NO_TEST=1
12 6	IN	CPU_CLK24M_NSSC_CLK_P	NO_TEST=1
12 6	IN	CPU_CLK100M_PCIBCLK_N	NO_TEST=1
12 6	IN	CPU_CLK100M_PCIBCLK_P	NO_TEST=1
12 6	IN	CPU_CLK100M_BCLK_N	NO_TEST=1
12 6	IN	CPU_CLK100M_BCLK_P	NO_TEST=1
87 12	IN	PCIE_CLK100M_SSD_N	NO_TEST=1
87 12	IN	PCIE_CLK100M_SSD_P	NO_TEST=1
87 77	IN	PCIE_CLK100M_SSD_LB_N	NO_TEST=1
87 77	IN	PCIE_CLK100M_SSD_LB_P	NO_TEST=1
115 18 12	IN	NC_ITPXDP_CLK100MN	NO_TEST=1
115 18 12	IN	NC_ITPXDP_CLK100MP	NO_TEST=1
35 12	IN	PCIE_CLK100M_AP_P	NO_TEST=1
35 12	IN	PCIE_CLK100M_AP_N	NO_TEST=1

MUX

89 5	IN	DP_INT_IG_ML_N<3..0>	NO_TEST=1
89 5	IN	DP_INT_IG_ML_P<3..0>	NO_TEST=1
89 5	IN	DP_INT_IG_AUX_N	NO_TEST=1
89 5	IN	DP_INT_IG_AUX_P	NO_TEST=1
99 89	IN	DP_INT_EG_ML_N<3..0>	NO_TEST=1
99 89	IN	DP_INT_EG_ML_P<3..0>	NO_TEST=1
99 89	IN	DP_INT_EG_AUX_N	NO_TEST=1
99 89	IN	DP_INT_EG_AUX_P	NO_TEST=1

DP MUX CRYSTAL

89	IN	DPMUX_UC_XTAL	NO_TEST=1
89	IN	DPMUX_UC_EXTAL	NO_TEST=1
89	IN	DPMUX_UC_EXTAL_R	NO_TEST=1
89	IN	DPMUX_UC_XTAL_R	NO_TEST=1

XTAL

	IN	GPU_XTAL_PU_OR_CAP	NO_TEST=1
	IN	NC_PCH_CLK24M_XTALOUT	NO_TEST=1
19	IN	SYSCLK_CLK24M_X2	NO_TEST=1
19	IN	SYSCLK_CLK24M_X2_R	NO_TEST=1
19	IN	SYSCLK_CLK24M_X1	NO_TEST=1
29 27	IN	TBT_X_XTAL25M_OUT	NO_TEST=1
29	IN	TBT_X_XTAL25M_OUT_R	NO_TEST=1
29 27	IN	TBT_X_XTAL25M_IN	NO_TEST=1
103 101	IN	TBT_T_XTAL25M_OUT	NO_TEST=1
103	IN	TBT_T_XTAL25M_OUT_R	NO_TEST=1
38	IN	SOC_XTAL_24M_O	NO_TEST=1
103 101	IN	TBT_T_XTAL25M_IN	NO_TEST=1
38	IN	SOC_XTAL_24M_I	NO_TEST=1
38	IN	SOC_XTAL_24M_O_R	NO_TEST=1
77	IN	SSD_CLKIN	NO_TEST=1
77	IN	SSD_CLKOUT	NO_TEST=1
77	IN	SSD_CLKOUT_R	NO_TEST=1
99 98	IN	GPU_XTAL_OUT	NO_TEST=1
99 98	IN	GPU_XTAL_OR_CLK_IN	NO_TEST=1
98	IN	GPU_XTAL_XTAL_OR_CLK	NO_TEST=1

MEM

26 22 7	IN	MEM_A_CAA<9..0>	NO_TEST=1
26 23 22 7	IN	MEM_A_CLK_P<1..0>	NO_TEST=1
26 23 22 7	IN	MEM_A_CLK_N<1..0>	NO_TEST=1
112 7	IN	MEM_A_DQ<63..0>	NO_TEST=1
112 7	IN	MEM_B_DQ<63..0>	NO_TEST=1
112 7	IN	MEM_A_DQS_P<7..0>	NO_TEST=1
112 7	IN	MEM_A_DQS_N<7..0>	NO_TEST=1
112 7	IN	MEM_B_DQS_P<7..0>	NO_TEST=1
112 7	IN	MEM_B_DQS_N<7..0>	NO_TEST=1
26 23 7	IN	MEM_A_CAB<9..0>	NO_TEST=1
26 24 7	IN	MEM_B_CAA<9..0>	NO_TEST=1
26 25 7	IN	MEM_B_CAB<9..0>	NO_TEST=1
26 25 24 7	IN	MEM_B_CLK_P<1..0>	NO_TEST=1
26 25 24 7	IN	MEM_B_CLK_N<1..0>	NO_TEST=1

WIFI

36	IN	50_0_ANT	NO_TEST=1
36	IN	50_1_ANT	NO_TEST=1
36	IN	50_2_ANT	NO_TEST=1
36	IN	50_0_COM	NO_TEST=1
36	IN	50_1_COM	NO_TEST=1
36	IN	50_2_COM	NO_TEST=1
36	IN	50_A_0_DIPLEXER	NO_TEST=1
36 35	IN	50_A_0_MATCH	NO_TEST=1
36	IN	50_G_0_DIPLEXER	NO_TEST=1
36 35	IN	50_G_0_MATCH	NO_TEST=1
36	IN	50_A_1_DIPLEXER	NO_TEST=1
36 35	IN	50_A_1_MATCH	NO_TEST=1
36	IN	50_G_1_DIPLEXER	NO_TEST=1
36 35	IN	50_G_1_MATCH	NO_TEST=1
36	IN	50_A_2_DIPLEXER	NO_TEST=1
36 35	IN	50_A_2_MATCH	NO_TEST=1
36	IN	50_G_2_DIPLEXER	NO_TEST=1
36 35	IN	50_G_2_MATCH	NO_TEST=1

USB-C T

106 101	IN	USBC_TA_D2R_P<2..1>	NO_TEST=1
106 101	IN	USBC_TA_D2R_N<2..1>	NO_TEST=1
106 101	IN	USBC_TA_R2D_C_P<2..1>	NO_TEST=1
106 101	IN	USBC_TA_R2D_C_N<2..1>	NO_TEST=1
104 101	IN	DP_TA_AUXCH_P	NO_TEST=1
104 101	IN	DP_TA_AUXCH_N	NO_TEST=1
101	IN	DP_TA_AUXCH_C_P	NO_TEST=1
101	IN	DP_TA_AUXCH_C_N	NO_TEST=1
106 101	IN	USBC_TB_D2R_P<2..1>	NO_TEST=1
106 101	IN	USBC_TB_D2R_N<2..1>	NO_TEST=1
106 101	IN	USBC_TB_R2D_C_P<2..1>	NO_TEST=1
106 101	IN	USBC_TB_R2D_C_N<2..1>	NO_TEST=1
105 101	IN	DP_TB_AUXCH_P	NO_TEST=1
105 101	IN	DP_TB_AUXCH_N	NO_TEST=1
101	IN	DP_TB_AUXCH_C_P	NO_TEST=1
101	IN	DP_TB_AUXCH_C_N	NO_TEST=1
85 83	IN	SSD_NAND_FH_DQ4	NO_TEST=1
85 83	IN	SSD_NAND_FH_DQ0	NO_TEST=1
85 83	IN	SSD_NAND_FH_DQS_P	NO_TEST=1
85 83	IN	SSD_NAND_FH_DQ5	NO_TEST=1
85 83	IN	SSD_NAND_FH_DQ6	NO_TEST=1
85 83	IN	SSD_NAND_FH_DQ7	NO_TEST=1
85 83	IN	SSD_NAND_FH_DQS_N	NO_TEST=1

NAND

85 82	IN	SSD_NAND_FA_DQ0	NO_TEST=1
85 82	IN	SSD_NAND_FA_DQ1	NO_TEST=1
85 82	IN	SSD_NAND_FA_DQ2	NO_TEST=1
85 82	IN	SSD_NAND_FA_DQ3	NO_TEST=1
85 82	IN	SSD_NAND_FA_DQ4	NO_TEST=1
85 82	IN	SSD_NAND_FA_DQ5	NO_TEST=1
85 82	IN	SSD_NAND_FA_DQ6	NO_TEST=1
85 82	IN	SSD_NAND_FA_DQ7	NO_TEST=1
85 82	IN	SSD_NAND_FA_DQS_N	NO_TEST=1
85 82	IN	SSD_NAND_FA_DQS_P	NO_TEST=1
85 82	IN	SSD_NAND_FB_DQ0	NO_TEST=1
85 82	IN	SSD_NAND_FB_DQ1	NO_TEST=1
85 82	IN	SSD_NAND_FB_DQ2	NO_TEST=1
85 82	IN	SSD_NAND_FB_DQ3	NO_TEST=1
85 82	IN	SSD_NAND_FB_DQ4	NO_TEST=1
85 82	IN	SSD_NAND_FB_DQ5	NO_TEST=1
85 82	IN	SSD_NAND_FB_DQ6	NO_TEST=1
85 82	IN	SSD_NAND_FB_DQ7	NO_TEST=1
85 82	IN	SSD_NAND_FB_DQS_N	NO_TEST=1
85 82	IN	SSD_NAND_FB_DQS_P	NO_TEST=1
85 82	IN	SSD_NAND_FC_DQ0	NO_TEST=1
85 82	IN	SSD_NAND_FC_DQ1	NO_TEST=1
85 82	IN	SSD_NAND_FC_DQ2	NO_TEST=1
85 82	IN	SSD_NAND_FC_DQ3	NO_TEST=1
85 82	IN	SSD_NAND_FC_DQ4	NO_TEST=1
85 82	IN	SSD_NAND_FC_DQ5	NO_TEST=1
85 82	IN	SSD_NAND_FC_DQ6	NO_TEST=1
85 82	IN	SSD_NAND_FC_DQ7	NO_TEST=1
85 82	IN	SSD_NAND_FC_DQS_N	NO_TEST=1
85 82	IN	SSD_NAND_FC_DQS_P	NO_TEST=1
85 82	IN	SSD_NAND_FD_DQ0	NO_TEST=1
85 82	IN	SSD_NAND_FD_DQ1	NO_TEST=1
85 82	IN	SSD_NAND_FD_DQ2	NO_TEST=1
85 82	IN	SSD_NAND_FD_DQ3	NO_TEST=1
85 82	IN	SSD_NAND_FD_DQ4	NO_TEST=1
85 82	IN	SSD_NAND_FD_DQ5	NO_TEST=1
85 82	IN	SSD_NAND_FD_DQ6	NO_TEST=1
85 82	IN	SSD_NAND_FD_DQ7	NO_TEST=1
85 82	IN	SSD_NAND_FD_DQS_N	
85 82	IN	SSD_NAND_FD_DQS_P	
85 83	IN	SSD_NAND_FE_DQ0	NO_TEST=1
85 83	IN	SSD_NAND_FE_DQ1	NO_TEST=1
85 83	IN	SSD_NAND_FE_DQ2	NO_TEST=1
85 83	IN	SSD_NAND_FE_DQ3	NO_TEST=1
85 83	IN	SSD_NAND_FE_DQ4	NO_TEST=1
85 83	IN	SSD_NAND_FE_DQ5	NO_TEST=1
85 83	IN	SSD_NAND_FE_DQ6	NO_TEST=1
85 83	IN	SSD_NAND_FE_DQ7	NO_TEST=1
85 83	IN	SSD_NAND_FE_DQS_N	NO_TEST=1
85 83	IN	SSD_NAND_FE_DQS_P	NO_TEST=1
85 83	IN	SSD_NAND_FF_DQ0	NO_TEST=1
85 83	IN	SSD_NAND_FF_DQ1	NO_TEST=1
85 83	IN	SSD_NAND_FF_DQ2	NO_TEST=1
85 83	IN	SSD_NAND_FF_DQ3	NO_TEST=1
85 83	IN	SSD_NAND_FF_DQ4	NO_TEST=1
85 83	IN	SSD_NAND_FF_DQ5	NO_TEST=1
85 83	IN	SSD_NAND_FF_DQ6	NO_TEST=1
85 83	IN	SSD_NAND_FF_DQ7	NO_TEST=1
85 83	IN	SSD_NAND_FF_DQS_N	NO_TEST=1
85 83	IN	SSD_NAND_FF_DQS_P	NO_TEST=1
85 83	IN	SSD_NAND_FG_DQ0	NO_TEST=1
85 83	IN	SSD_NAND_FG_DQ2	NO_TEST=1
85 83	IN	SSD_NAND_FG_DQ3	NO_TEST=1
85 83	IN	SSD_NAND_FG_DQ4	NO_TEST=1
85 83	IN	SSD_NAND_FG_DQ5	NO_TEST=1
85 83	IN	SSD_NAND_FG_DQ6	NO_TEST=1
85 83	IN	SSD_NAND_FG_DQ7	NO_TEST=1
85 83	IN	SSD_NAND_FG_DQS_N	NO_TEST=1
85 83	IN	SSD_NAND_FG_DQS_P	NO_TEST=1
85 83	IN	SSD_NAND_FH_DQ1	NO_TEST=1
85 83	IN	SSD_NAND_FH_DQ2	NO_TEST=1
85 83	IN	SSD_NAND_FH_DQ3	NO_TEST=1

SYNC_MASTER=X363_SANXOC SYNC_DATE=04/14/2016

PAGE TITLE

ICT & FCT 1

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MESA CONNECTOR

Page refs	Signal	Property
45	PP3V0_MESA_CONN	FUNC_TEST=TRUE
45	MESA_SPI_MISO_CONN	FUNC_TEST=TRUE
45	MESA_SNSR_INT_CONN	FUNC_TEST=TRUE
45	MESA_BOOST_EN_CONN	FUNC_TEST=TRUE
45 37	MESA_I2C_SDA	FUNC_TEST=TRUE
45 37	MESA_I2C_SCL	FUNC_TEST=TRUE
45	PP1V8_MESA_CONN	FUNC_TEST=TRUE
45	MESA_SPI_MOSI_CONN	FUNC_TEST=TRUE
45	MENU_KEY_L	FUNC_TEST=TRUE
45	MESA_SPI_CLK_CONN	FUNC_TEST=TRUE
45	PP16V0_MESA_CONN	FUNC_TEST=TRUE
	GND	

SPI ROM

Page refs	Signal	Property
114 109	PP3V3_G3H	FUNC_TEST=TRUE
57	SPI_ALT_IO0_MOSI	FUNC_TEST=TRUE
57	SPI_ALT_IO1_MISO	FUNC_TEST=TRUE
57	SPI_ALT_IO2_WP_L	FUNC_TEST=TRUE
57	SPI_ALT_IO3_HOLD_L	FUNC_TEST=TRUE
76 64 57 48 29 114	SMC_RESET_L	FUNC_TEST=TRUE
57	SPI_ALT_CLK	FUNC_TEST=TRUE
57	SPI_ALT_CS_L	FUNC_TEST=TRUE
57 15	SPIROM_USE_MLB	FUNC_TEST=TRUE
57 47 46	SMC_TMS	FUNC_TEST=TRUE
57 47 46	SMC_TCK	FUNC_TEST=TRUE
	GND	

AUDIO AMP

Page refs	Signal	Property
61	SPKRCONN_TR_OUT_POS	FUNC_TEST=TRUE
61	SPKRCONN_TR_OUT_NEG	FUNC_TEST=TRUE
61	SPKRCONN_WR_OUT_POS	FUNC_TEST=TRUE
61	SPKRCONN_WR_OUT_NEG	FUNC_TEST=TRUE
60	SPKRCONN_TL_OUT_POS	FUNC_TEST=TRUE
60	SPKRCONN_TL_OUT_NEG	FUNC_TEST=TRUE
60	SPKRCONN_WL_OUT_POS	FUNC_TEST=TRUE
60	SPKRCONN_WL_OUT_NEG	FUNC_TEST=TRUE
61 58	SPKR_ID0	FUNC_TEST=TRUE
	GND	FUNC_TEST=

DFR Touch Conn

Page refs	Signal	Note	Property
42	DFR_TOUCH_LID		FUNC_TEST=TRUE
42 38	DFR_TOUCH_GPIO2		FUNC_TEST=TRUE
42 37	DFR_TOUCH_SPI_CS_L		FUNC_TEST=TRUE
42	DFR_TOUCH_SPI_MOSI_R		FUNC_TEST=TRUE
42 38 37	DFR_TOUCH_ROM_I2C_SCL		FUNC_TEST=TRUE
42 38 37	DFR_TOUCH_ROM_I2C_SDA		FUNC_TEST=TRUE
42 37	DFR_TOUCH_RESET_L		FUNC_TEST=TRUE
114 42 37	PP1V8_S0SW_DFR	X2	FUNC_TEST=TRUE
110	PP5V_S0_T139		FUNC_TEST=TRUE
42 38	DFR_TOUCH_PANEL_DETECT		FUNC_TEST=TRUE
114 42 38	DFR_DISP_VSYNC		FUNC_TEST=TRUE
42	DFR_TOUCH_SPI_MISO_R		FUNC_TEST=TRUE
42	DFR_TOUCH_SPI_CLK_R		FUNC_TEST=TRUE
42 38	DFR_TOUCH_INT_L		FUNC_TEST=TRUE
42 38	DFR_CLKIN_RESET_L		FUNC_TEST=TRUE
42 38	DFR_TOUCH_ROM_WC		FUNC_TEST=TRUE
	GND	X4	

DFR Disp Conn

Page refs	Signal	Note	Property
114 42 38	DFR_DISP_VSYNC		FUNC_TEST=TRUE
42 38	DFR_DISP_TE		FUNC_TEST=TRUE
42 38	DFR_DISP_INT		FUNC_TEST=TRUE
42	DFR_DISP_RESET_L		FUNC_TEST=TRUE
42	PP3V3_S0SW_DFR	X3	FUNC_TEST=TRUE
42 38	MIPID_CLK_P		FUNC_TEST=TRUE
42 38	MIPID_CLK_N		FUNC_TEST=TRUE
42 38	MIPID_DATA_P		FUNC_TEST=TRUE
42 38	MIPID_DATA_N		FUNC_TEST=TRUE
114 42 37	PP1V8_S0SW_DFR	X2	FUNC_TEST=TRUE
42 38 37	DFRDRV_I2C_SCL		FUNC_TEST=TRUE
42 38 37	DFRDRV_I2C_SDA		FUNC_TEST=TRUE
	GND	X6	

KBD CONNECTOR

Page refs	Signal	Note	Property
43	GND_FAN	X2	FUNC_TEST=TRUE
43	PP5V_S0_FAN_CONN	X2	FUNC_TEST=TRUE
115 56 43	FAN_LT_TACH		FUNC_TEST=TRUE
115 56 43	FAN_LT_PWM		FUNC_TEST=TRUE
110	PP5V_S0_KBD	X2	FUNC_TEST=TRUE
114 109	PP3V3_G3H		FUNC_TEST=TRUE
114 43	KBD_BLC_GSSOUT		FUNC_TEST=TRUE
114 43	KBD_BLC_GSLAT		FUNC_TEST=TRUE
110 103 29	PP3V3_S4		FUNC_TEST=TRUE
114 43	KBD_BLC_GSSIN		FUNC_TEST=TRUE
43	KBD_BLC_XBLANK		FUNC_TEST=TRUE
115 56 43	FAN_RT_TACH		FUNC_TEST=TRUE
115 56 43	FAN_RT_PWM		FUNC_TEST=TRUE
114 43	KBD_I2C_SDA		FUNC_TEST=TRUE
114 43	KBD_INT_L		FUNC_TEST=TRUE
114 43	KBD_I2C_SCL		FUNC_TEST=TRUE
114 48 43	SMC_LSOC_RST_L		FUNC_TEST=TRUE
114 43	KBD_BLC_GSSCK		FUNC_TEST=TRUE
	GND	X5	

TPAD CONNECTOR

Page refs	Signal	Note	Property
114 43	KBD_I2C_SCL		FUNC_TEST=TRUE
114 43	KBD_I2C_SDA		FUNC_TEST=TRUE
114 43	KBD_INT_L		FUNC_TEST=TRUE
49 46	SMBUS_SMC_3_SDA		FUNC_TEST=TRUE
49 46	SMBUS_SMC_3_SCL		FUNC_TEST=TRUE
110	PP3V3_S4_TPAD		FUNC_TEST=TRUE
43	PP5V_S4_TPAD_CONN		FUNC_TEST=TRUE
43	ACT_GND	X4	FUNC_TEST=TRUE
43	PPVIN_S4_TPAD_FUSE	X4	FUNC_TEST=TRUE
43 13	TPAD_SPI_CLK		FUNC_TEST=TRUE
43	TPAD_SPI_IF_EN_CONN		FUNC_TEST=TRUE
43 13	TPAD_SPI_MISO		FUNC_TEST=TRUE
43	TPAD_SPI_CS_L_CONN		FUNC_TEST=TRUE
43 13	TPAD_SPI_MOSI		FUNC_TEST=TRUE
43	TPAD_SPI_INT_L_CONN		FUNC_TEST=TRUE
48 46	SMC_ACTUATOR_DISABLE_L		FUNC_TEST=TRUE
48 47 46	SMC_PME_S4_WAKE_L		FUNC_TEST=TRUE
48 47 43 42	SMC_LID		FUNC_TEST=TRUE
114 43	KBD_BLC_GSLAT		FUNC_TEST=TRUE
114 43	KBD_BLC_GSSCK		FUNC_TEST=TRUE
114 43	KBD_BLC_GSSOUT		FUNC_TEST=TRUE
46 43	SMC_VIBE_L		FUNC_TEST=TRUE
114 43	KBD_BLC_GSSIN		FUNC_TEST=TRUE
	GND	X3	

eDP

Page refs	Signal	Note	Property
116 76 75	PPVOUT_S0_LCDBKLT		FUNC_TEST=TRUE
76	PP3V3_S0SW_LCD	X2	FUNC_TEST=TRUE
76	EDP_AUXCH_C_N		FUNC_TEST=TRUE
76	EDP_AUXCH_C_P		FUNC_TEST=TRUE
111 76	EDP_INT_ML_N<0>		FUNC_TEST=TRUE
111 76	EDP_INT_ML_P<0>		FUNC_TEST=TRUE
111 76	EDP_INT_ML_N<1>		FUNC_TEST=TRUE
111 76	EDP_INT_ML_P<1>		FUNC_TEST=TRUE
111 76	EDP_INT_ML_N<2>		FUNC_TEST=TRUE
111 76	EDP_INT_ML_P<2>		FUNC_TEST=TRUE
111 76	EDP_INT_ML_N<3>		FUNC_TEST=TRUE
111 76	EDP_INT_ML_P<3>		FUNC_TEST=TRUE
38	MIPIC_CLK_N		FUNC_TEST=TRUE
38	MIPIC_CLK_P		FUNC_TEST=TRUE
76	PP5V_S0SW_LCD		FUNC_TEST=TRUE
76 38	PP5V_S0_ALSCAM_F		FUNC_TEST=TRUE
76 42	I2C_ALS_SDA		FUNC_TEST=TRUE
76 42	I2C_ALS_SCL		FUNC_TEST=TRUE
76 38 37	I2C_CAM_SCL		FUNC_TEST=TRUE
76 38 37	I2C_CAM_SDA		FUNC_TEST=TRUE
111 76	I2C_BKLT_SDA		FUNC_TEST=TRUE
111 76	I2C_BKLT_SCL		FUNC_TEST=TRUE
49 46	SMBUS_SMC_0_S0_SDA		FUNC_TEST=TRUE
49 46	SMBUS_SMC_0_S0_SCL		FUNC_TEST=TRUE
76 48	BKLT_PWM_TCON2MLB		FUNC_TEST=TRUE
76 20	BKLT_PWM_MLB2TCON		FUNC_TEST=TRUE
89 76	LCD_FSS		FUNC_TEST=TRUE
76 15	LCD_IRQ_L		FUNC_TEST=TRUE
76	BUF_EDP_PANEL_PWR_EN		FUNC_TEST=TRUE
89 76	DP_INT_HPD		FUNC_TEST=TRUE
	GND	X3	
76 49	SMBUS_SMC_0_S0_SCL		FUNC_TEST=TRUE
76 49	SMBUS_SMC_0_S0_SDA		FUNC_TEST=TRUE
38	MIPIC_DATA_P		FUNC_TEST=TRUE
38	MIPIC_DATA_N		FUNC_TEST=TRUE

AUDIO JACK

Page refs	Signal	Note	Property
62	AUD_CONN_HP_LEFT		FUNC_TEST=TRUE
62	AUD_CONN_HP_RIGHT		FUNC_TEST=TRUE
62	AUD_CONN_RING2		FUNC_TEST=TRUE
62	AUD_CONN_SLEEVE		FUNC_TEST=TRUE
62	AUD_CONN_HP_SENSE_L		FUNC_TEST=TRUE
62	AUD_CONN_HP_SENSE_R		FUNC_TEST=TRUE
62	AUD_CONN_TIP_SENSE		FUNC_TEST=TRUE
62	AUD_CONN_SLEEVE_XW		FUNC_TEST=TRUE
62	AUD_CONN_RING2_XW		FUNC_TEST=TRUE
	GND	X2	

BATTERY TUBA

Page refs	Signal	Note	Property
64 63	PPVBAT_G3H_CONN	X7	FUNC_TEST=TRUE
49 46	SMBUS_SMC_5_G3_SCL		FUNC_TEST=TRUE
49 46	SMBUS_SMC_5_G3_SDA		FUNC_TEST=TRUE
63	TP_BMON_IOUT		FUNC_TEST=TRUE
64 50	CHGR_AMON		FUNC_TEST=TRUE
64 50	CHGR_BMON		FUNC_TEST=TRUE
63	SYS_DETECT_L		FUNC_TEST=TRUE
	GND	X5	
114 48 43	SMC_LSOC_RST_L		FUNC_TEST=TRUE
64	TBA_COMP		FUNC_TEST=TRUE
64	TBA_VDDA		FUNC_TEST=TRUE
64	TBA_LX1		FUNC_TEST=TRUE
64	TBA_LX2		FUNC_TEST=TRUE
	GND	X2	
64	PPVBAT_G3H_CHGR_REG	X5	FUNC_TEST=TRUE
116 64 63	PPDCIN_G3H_CHGR	X5	FUNC_TEST=TRUE

USB_C

TP_UPC_XA_SWD_DATA ------------------------> TP3001
TP_UPC_XA_SWD_CLK ------------------------> TP3002
TP_UPC_XB_SWD_DATA ------------------------> TP3003
TP_UPC_XB_SWD_CLK ------------------------> TP3004

Page refs	Signal	Note	Property
104 103	TP_UPC_TA_DBG_UART_TX		FUNC_TEST=TRUE
104 103	TP_UPC_TA_DBG_UART_RX		FUNC_TEST=TRUE
105 103	TP_UPC_TB_DBG_UART_TX		FUNC_TEST=TRUE
105 103	TP_UPC_TB_DBG_UART_RX		FUNC_TEST=TRUE
30 29	UPC_XA_DBG_UART_TX		FUNC_TEST=TRUE
30 29	UPC_XA_DBG_UART_RX		FUNC_TEST=TRUE
31 29	TP_UPC_XB_DBG_UART_TX		FUNC_TEST=TRUE
31 29	TP_UPC_XB_DBG_UART_RX		FUNC_TEST=TRUE
116 115 106	PP20V_USBC_TB_VBUS_CONN	X5	FUNC_TEST=TRUE
116 115 106	PP20V_USBC_TA_VBUS_CONN	X5	FUNC_TEST=TRUE
	GND	X5	
116 115 32	PP20V_USBC_XB_VBUS_CONN	X4	FUNC_TEST=TRUE
116 115 32	PP20V_USBC_XA_VBUS_CONN	X5	FUNC_TEST=TRUE
	GND	X5	

SSD DEBUG CONNECTOR

Page refs	Signal	Property
115 87 77	SSD_BOOT_LB_L	FUNC_TEST=TRUE
80 77	SSD_BOOT_LB_L	FUNC_TEST=TRUE
103 86 80	SSD_DEBUG_I2C_CLK_CONN	FUNC_TEST=TRUE
103 86 80	SSD_DEBUG_I2C_DAT_CONN	FUNC_TEST=TRUE
80 77 48	SMC_OOB1_R2D_L	FUNC_TEST=TRUE
80 77 48	SMC_OOB1_D2R_L	FUNC_TEST=TRUE
83 82 81 80 78 77 15 84	PP1V8_SSD_FMC	FUNC_TEST=TRUE
	GND	

MIC

Page refs	Signal	Property
58	DMIC1_CLK	FUNC_TEST=TRUE
58	DMIC1_DATA	FUNC_TEST=TRUE
58	DMIC2_CLK	FUNC_TEST=TRUE
58	DMIC2_DATA	FUNC_TEST=TRUE
109 61	PP1V8_S0	FUNC_TEST=TRUE
	GND	

USB-C PROBE BLOCK TESTING

Page refs	Signal	Property	Test point
32	TP_J3300_P2	FUNC_TEST=TRUE	TPAC580
32	TP_J3300_P56	FUNC_TEST=TRUE	TPAC581
106	TP_JB500_P2		TPAC582
106	TP_JB500_P56	FUNC_TEST=TRUE	TPAC583

ADDITIONAL TPs

Page refs	Signal	Property	Test point
110	PP3V3_S5	FUNC_TEST=TRUE	TPAC584
110	PP3V3_SUS	FUNC_TEST=TRUE	TPAC585

Wifi & SSD fixture Test Points

(row,col)=(4,2) Diameter=0.6mm Pitch=1mm

Right Side - Top Layer

Page refs	Signal	Test point
	GND	TPAC528
80 77	SSD_JTAG_TMS	TPAC519
80 77	SSD_JTAG_TCK	TPAC520
80 77	SSD_JTAG_TDI	TPAC521
80 77	SSD_JTAG_TDO	TPAC522
86 77	SSD_DEBUG_I2C_CLK	TPAC523
86 77	SSD_DEBUG_I2C_DAT	TPAC524
84 77	SSD_PGOOD_L	TPAC535

(row,col)=(2,6) Diameter=0.6mm Pitch=1mm

Left Side - Top Layer

Page refs	Signal	Test point
50 114 116 29 64	PPDCIN_G3H	TPAC500
50 114 116 29 64	PPDCIN_G3H	TPAC501
50 114 116 29 64	PPDCIN_G3H	TPAC502
50 114 116 29 64	PPDCIN_G3H	TPAC503
	GND	TPAC504
	GND	TPAC505
	GND	TPAC506
	GND	TPAC507
	GND (TRUE)	TPAC529
64	HPWR_EN_L	TPAC512
110	PP3V3_S0	TPAC536
114 109	PP3V3_G3H	TPAC518

(row,col)=(5,5) Diameter=0.6mm Pitch=1mm

Middle - Top Layer

Page refs	Signal	Test point
46 48 45 47	SMC_ONOFF_L	TPAC517
	GND	TPAC538
76 48 64 114 29 57	SMC_RESET_L	TPAC539
	GND	TPAC527
14	USB3_TEST_D2R_N	TPAC510
14	USB3_TEST_D2R_P	TPAC511
	GND	TPAC595
	GND	TPAC596
84 78	PP1V0_SSD_CORE	TPAC598
109	PPVCC_S0_CPU	TPAC597
109	PPBUS_G3H	TPAC599
14	USB3_TEST_R2D_N	TPAC525
14	USB3_TEST_R2D_P	TPAC526
20 36 15 35	AP_RESET_L	TPAC537
14	USB_TEST_P	TPAC530
14	USB_TEST_N	TPAC531
20 115 14 87	SSD_RESET_L	TPAC532
46 12 73	PM_PCH_SYS_PWROK	TPAC533
87 14 115	SSD_PWR_EN	TPAC534
46 29 47	SMC_DEBUGPRT_TX_L	TPAC508
46 29 47	SMC_DEBUGPRT_RX_L	TPAC509
87 115 15 101	SSD_BOOT_L	TPAC513
73 20 46 89 70 12 27 76	PM_SLP_S3_L	TPAC514
48	SMC_DEV_SUPPLY_R_L	TPAC515
20 12 35	PLT_RST_L	TPAC516

All test points: pin 1, TP-P6, A.

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OTHER TEST POINTS / NC

NC with No Testpoint Property

13	NC_CLINK_CLK	1	TRUE	NC_CLINK_CLK	
13	NC_CLINK_DATA	1	TRUE	NC_CLINK_DATA	
13	NC_CLINK_RESET_L	1	TRUE	NC_CLINK_RESET_L	
113 18 12	NC_ITPXDP_CLK100MN	1	TRUE	NC_ITPXDP_CLK100MN	
113 18 12	NC_ITPXDP_CLK100MP	1	TRUE	NC_ITPXDP_CLK100MP	
13	NC_HDA_SDIN1	1	TRUE	NC_HDA_SDIN1	
TP	1	NC_SPI_SMC_MOSI			48
TP	1	NC_SPI_SMC_MISO			48
TP	1	NC_SPI_SMC_CS_L			48
TP	1	NC_SPI_SMC_CLK			48
TP		NC_PCH_CLK32K_RTCX2			20

FAN Test Points

TP	TRUE	FAN_LT_PWM	43 56 114
TP	TRUE	FAN_LT_TACH	43 56 114
TP	TRUE	PP5V_S0	38 110 115
TP	TRUE	FAN_RT_PWM	43 56 114
TP	TRUE	FAN_RT_TACH	43 56 114
TP	TRUE	PP5V_S0	38 110 115

XDP Test-Points

TP	TRUE	XDP_CPU_TCK	6 18
TP	TRUE	XDP_PCH_TCK	13 18
TP	TRUE	XDP_CPU_TDI	6 18
TP	TRUE	XDP_CPU_TDO	6 18
TP	TRUE	XDP_CPU_TRST_L	6 13 18
TP	TRUE	XDP_CPU_TMS	6 18
TP	TRUE	XDP_PCH_TMS	13 18
TP	TRUE	XDP_PCH_TDI	13 18
TP	TRUE	XDP_PCH_TDO	13 18
TP	TRUE	XDP_CPU_PREQ_L	6 13 18
TP	TRUE	XDP_CPU_PRDY_L	6 13 18
TP	TRUE	PM_RSMRST_L	12 18 46 73
TP	TRUE	PM_PCH_PWROK	12 70
TP	TRUE	PM_SYSRST_L	12 18 46
TP	TRUE	CPU_CFG<3>	6 18

CPU (Refer to CPU pages)

CPU_DC_B2_C1	---------->	TP0501
CPU_DC_B38_C38	---------->	TP0502
CPU_DC_BR2_BR1	---------->	TP0503
CPU_DC_C1_B2	---------->	TP0504
CPU_DC_C38_B38	---------->	TP0505
CPU_DC_BR1_BR2	---------->	TP0610
CPU_DC_BR38_BT36	---------->	TP0900
CPU_DC_BT36_BR38	---------->	TP0901

PCH (Refer to PCH pages)

XDP_PCH_OBSDATA_A0	---------->	TP1883
XDP_PCH_OBSDATA_A1	---------->	TP1884
XDP_PCH_OBSDATA_A2	---------->	TP1870
XDP_PCH_OBSDATA_A3	---------->	TP1871
XDP_PCH_OBSDATA_B0	---------->	TP1872
XDP_PCH_OBSDATA_B1	---------->	TP1885
XDP_PCH_OBSDATA_B2	---------->	TP1886
XDP_PCH_OBSDATA_B3	---------->	TP1887
XDP_PCH_OBSDATA_D0	---------->	TP1877
XDP_PCH_OBSDATA_D1	---------->	TP1878
XDP_PCH_OBSDATA_D2	---------->	TP1879
XDP_PCH_OBSDATA_D3	---------->	TP1880
XDP_PCH_OBSFN_C0	---------->	TP1882
XDP_BPM_L<0>	---------->	TP1800
XDP_BPM_L<1>	---------->	TP1801
XDP_BPM_L<2>	---------->	TP1802
XDP_BPM_L<3>	---------->	TP1803
NC_USB_EXTA_OC_L	---------->	TP1873
NC_USB_EXTB_OC_L	---------->	TP1874
NC_USB_EXTC_OC_L	---------->	TP1875
NC_USB_EXTD_OC_L	---------->	TP1876

TPs on BOTTOM to check USB-C Instalation

TP	USBC_XA_SBU1	FUNC_TEST=TRUE	30 32
TP	USBC_XB_SBU1	FUNC_TEST=TRUE	31 32
TP	USBC_XA_SBU2	FUNC_TEST=TRUE	30 32
TP	USBC_XB_SBU2	FUNC_TEST=TRUE	31 32
TP	USBC_TA_SBU1	FUNC_TEST=TRUE	104 106
TP	USBC_TB_SBU1	FUNC_TEST=TRUE	105 106
TP	USBC_TA_SBU2	FUNC_TEST=TRUE	104 106
TP	USBC_TB_SBU2	FUNC_TEST=TRUE	105 106
TP	PP20V_USBC_XA_VBUS_CONN	FUNC_TEST=TRUE	32 114 116
TP	PP20V_USBC_XB_VBUS_CONN	FUNC_TEST=TRUE	32 114 116
TP	PP20V_USBC_TA_VBUS_CONN	FUNC_TEST=TRUE	106 114 116
TP	PP20V_USBC_TB_VBUS_CONN	FUNC_TEST=TRUE	106 114 116

TPs to check LifeBoat Instalation

TP	PP3V3_S5_POLARIS	FUNC_TEST=TRUE	84 87
TP	PP3V3_S5	FUNC_TEST=TRUE	110
TP	SSD_PWR_EN	FUNC_TEST=TRUE	14 87 114
TP	SSD_PWR_LB_EN	FUNC_TEST=TRUE	84 87
TP	SSD_BOOT_L	FUNC_TEST=TRUE	15 87 114
TP	SSD_BOOT_LB_L	FUNC_TEST=TRUE	77 87 114
TP	SSD_RESET_L	FUNC_TEST=TRUE	14 20 87 114
TP	SSD_RESET_LB_L	FUNC_TEST=TRUE	77 87
TP	SSD_CLKREQ_L	FUNC_TEST=TRUE	20 87
TP	SSD_CLKREQ_LB_L	FUNC_TEST=TRUE	77 87

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
131S00041	6	CAP,CER,12PF,5%,100V,C0G,0402	CC784,CC785,CC786,CC787,CC788	CRITICAL	

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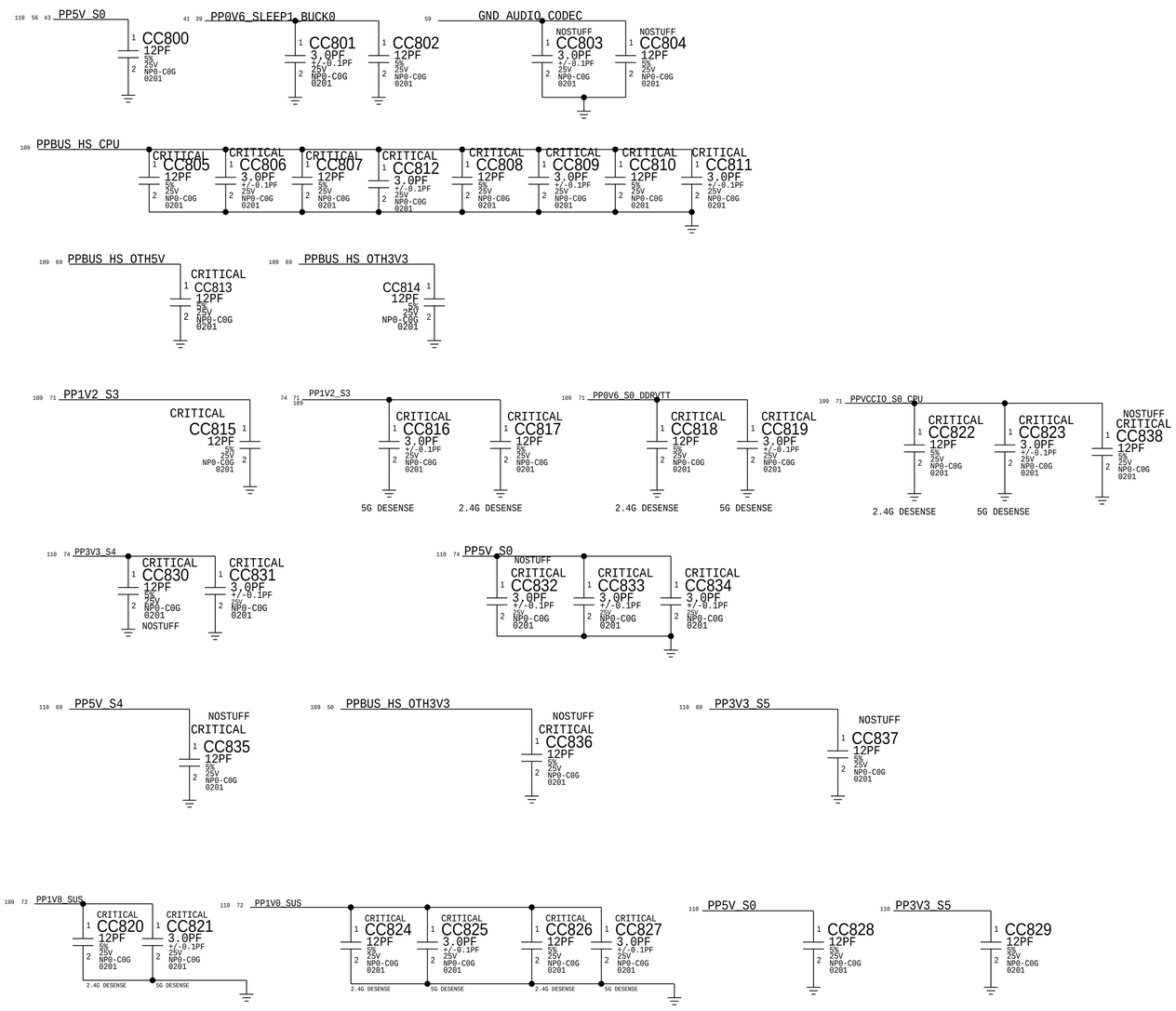

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Apple Inc.

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REVISION 10.0.0
BRANCH dvt-fab10
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DRAWING NUMBER	051-00647
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BOM Variants

44 ULA Configs

BOM NUMBER	BOM NAME	BOM OPTIONS
639-02212	MLB,2.6G,MC-16,ULA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02120	MLB,2.6G,MC-16,ULA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02591	MLB,2.6G,MC-16,ULA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-02214	MLB,2.6G,MC-16,ULA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-02587	MLB,2.6G,SM-16,ULA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02116	MLB,2.6G,SM-16,ULA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02589	MLB,2.6G,SM-16,ULA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-02586	MLB,2.6G,SM-16,ULA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01615	MLB,2.7G,MC-16,ULA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02592	MLB,2.7G,MC-16,ULA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01614	MLB,2.7G,MC-16,ULA-MC,SSD-512,X36G3	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01603	MLB,2.7G,SM-16,ULA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02594	MLB,2.7G,SM-16,ULA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01602	MLB,2.7G,SM-16,ULA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01639	MLB,2.9G,MC-16,ULA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-01637	MLB,2.9G,MC-16,ULA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02596	MLB,2.9G,MC-16,ULA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01638	MLB,2.9G,MC-16,ULA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01627	MLB,2.9G,SM-16,ULA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-01625	MLB,2.9G,SM-16,ULA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02598	MLB,2.9G,SM-16,ULA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01626	MLB,2.9G,SM-16,ULA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-02154	MLB,2.6G,MC-16,ULA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02119	MLB,2.6G,MC-16,ULA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02590	MLB,2.6G,MC-16,ULA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-02213	MLB,2.6G,MC-16,ULA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-02211	MLB,2.6G,SM-16,ULA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02115	MLB,2.6G,SM-16,ULA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02588	MLB,2.6G,SM-16,ULA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-02585	MLB,2.6G,SM-16,ULA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01612	MLB,2.7G,MC-16,ULA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02593	MLB,2.7G,MC-16,ULA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01611	MLB,2.7G,MC-16,ULA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01600	MLB,2.7G,SM-16,ULA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02595	MLB,2.7G,SM-16,ULA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01599	MLB,2.7G,SM-16,ULA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01636	MLB,2.9G,MC-16,ULA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-01634	MLB,2.9G,MC-16,ULA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02597	MLB,2.9G,MC-16,ULA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01635	MLB,2.9G,MC-16,ULA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01624	MLB,2.9G,SM-16,ULA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-01622	MLB,2.9G,SM-16,ULA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02599	MLB,2.9G,SM-16,ULA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01623	MLB,2.9G,SM-16,ULA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB

36 PROA Configs

BOM NUMBER	BOM NAME	BOM OPTIONS
639-02655	MLB,2.7G,MC-16,PROA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02656	MLB,2.7G,MC-16,PROA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02654	MLB,2.7G,MC-16,PROA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02664	MLB,2.7G,SM-16,PROA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02665	MLB,2.7G,SM-16,PROA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02663	MLB,2.7G,SM-16,PROA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02673	MLB,2.9G,MC-16,PROA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02674	MLB,2.9G,MC-16,PROA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02672	MLB,2.9G,MC-16,PROA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02682	MLB,2.9G,SM-16,PROA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02683	MLB,2.9G,SM-16,PROA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02681	MLB,2.9G,SM-16,PROA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02652	MLB,2.7G,MC-16,PROA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02653	MLB,2.7G,MC-16,PROA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02651	MLB,2.7G,MC-16,PROA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02661	MLB,2.7G,SM-16,PROA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02662	MLB,2.7G,SM-16,PROA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02660	MLB,2.7G,SM-16,PROA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02670	MLB,2.9G,MC-16,PROA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02671	MLB,2.9G,MC-16,PROA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02669	MLB,2.9G,MC-16,PROA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02679	MLB,2.9G,SM-16,PROA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02680	MLB,2.9G,SM-16,PROA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02678	MLB,2.9G,SM-16,PROA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02649	MLB,2.7G,MC-16,PROA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02650	MLB,2.7G,MC-16,PROA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02648	MLB,2.7G,MC-16,PROA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02658	MLB,2.7G,SM-16,PROA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02659	MLB,2.7G,SM-16,PROA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02657	MLB,2.7G,SM-16,PROA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02667	MLB,2.9G,MC-16,PROA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02668	MLB,2.9G,MC-16,PROA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02666	MLB,2.9G,MC-16,PROA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02676	MLB,2.9G,SM-16,PROA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02677	MLB,2.9G,SM-16,PROA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02675	MLB,2.9G,SM-16,PROA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB

BOM Variants, Power/Socket Configs

BOM NUMBER	BOM NAME	BOM OPTIONS
639-01966	PCBA,MLB,NONE,SM-16,FB4-SM,S256,X363	BASE_BOM,DEVEL_BOM,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,SSD_CONFIG:256GB
639-01967	PCBA,MLB,SKT,VDDC,SM-16,FB4-SM,S256,X363	BASE_BOM,DEVEL_BOM,STARDUST:VDDC,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,SSD_CONFIG:256GB
639-01968	PCBA,MLB,SKT,MVDD,SM-16,FB4-SM,S256,X363	BASE_BOM,DEVEL_BOM,STARDUST:VDDC2_MVDD,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,SSD_CONFIG:256GB
639-01969	PCBA,MLB,SKT,CPU,SM-16,FB4-SM,S256,X363	BASE_BOM,DEVEL_BOM,CPU_SKL:SOCKET,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,SSD_CONFIG:256GB

SYNC_MASTER=J80_MLB SYNC_DATE=07/23/2015

PAGE TITLE
639 BOM Configuration

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

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BOM Variants

48 LEA Configs

BOM NUMBER	BOM NAME	BOM OPTIONS
639-02621	MLB,2.6G,MC-16,LEA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02618	MLB,2.6G,MC-16,LEA-HY,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02622	MLB,2.6G,MC-16,LEA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02620	MLB,2.6G,MC-16,LEA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02608	MLB,2.6G,SM-16,LEA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02602	MLB,2.6G,SM-16,LEA-HY,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02611	MLB,2.6G,SM-16,LEA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02605	MLB,2.6G,SM-16,LEA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02645	MLB,2.9G,MC-16,LEA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02643	MLB,2.9G,MC-16,LEA-HY,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02646	MLB,2.9G,MC-16,LEA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02644	MLB,2.9G,MC-16,LEA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02633	MLB,2.9G,SM-16,LEA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02631	MLB,2.9G,SM-16,LEA-HY,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02634	MLB,2.9G,SM-16,LEA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02632	MLB,2.9G,SM-16,LEA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02647	MLB,2.6G,MC-16,LEA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02616	MLB,2.6G,MC-16,LEA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02619	MLB,2.6G,MC-16,LEA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02617	MLB,2.6G,MC-16,LEA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02607	MLB,2.6G,SM-16,LEA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02601	MLB,2.6G,SM-16,LEA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02610	MLB,2.6G,SM-16,LEA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02604	MLB,2.6G,SM-16,LEA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02641	MLB,2.9G,MC-16,LEA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02639	MLB,2.9G,MC-16,LEA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02642	MLB,2.9G,MC-16,LEA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02640	MLB,2.9G,MC-16,LEA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02629	MLB,2.9G,SM-16,LEA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02627	MLB,2.9G,SM-16,LEA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02630	MLB,2.9G,SM-16,LEA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02628	MLB,2.9G,SM-16,LEA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02614	MLB,2.6G,MC-16,LEA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02612	MLB,2.6G,MC-16,LEA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02615	MLB,2.6G,MC-16,LEA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02613	MLB,2.6G,MC-16,LEA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02606	MLB,2.6G,SM-16,LEA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02600	MLB,2.6G,SM-16,LEA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02609	MLB,2.6G,SM-16,LEA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02603	MLB,2.6G,SM-16,LEA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02637	MLB,2.9G,MC-16,LEA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02635	MLB,2.9G,MC-16,LEA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02638	MLB,2.9G,MC-16,LEA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02636	MLB,2.9G,MC-16,LEA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02625	MLB,2.9G,SM-16,LEA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02623	MLB,2.9G,SM-16,LEA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02626	MLB,2.9G,SM-16,LEA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02624	MLB,2.9G,SM-16,LEA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB

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PAGE TITLE
639 BOM Configuration 2

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Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
740S0144	740S0118		ALL		
740S00003	740S0135		ALL		
376S1089	376S1128		ALL		
376S1080	376S0820		ALL		
376S00086	376S0761		ALL		
376S00074	376S0855		ALL		
376S00014	376S0761		ALL		
372S0186	372S0185		ALL		
371S0713	371S0558		ALL		
311S00060	311S0273		ALL		
311S00004	311S0370		ALL		
155S0914	155S0897		ALL		
155S0694	155S0387		ALL		
155S0660	155S0513		ALL		
155S00154	155S0398		ALL		
155S00007	155S0667		ALL		
138S0863	138S0853		ALL		
138S0775	138S0860		ALL		<rdar://problem/23155097> for IG <rdar://problem/23564467> for EG
138S0703	138S0648		ALL		<rdar://problem/23118884> for IG <rdar://problem/> for EG
132S00064	132S0409		ALL		
128S0325	128S0397		ALL		
128S00029	128S00007		ALL		
128S00026	128S00011		ALL		
128S00070	128S00007		ALL		<rdar://problem/25329164>
128S00009	128S00007		ALL		
107S0249	107S0251		ALL		
107S00071	107S00053		ALL		
107S00070	107S0085		ALL		
107S00033	107S00034		ALL		BLC
107S00015	107S00011		ALL		
376S1106	376S0678		ALL	Fairchild alt to Vishay	BLC
138S0738	138S1101		ALL	Samsung alt to Murata	
138S0846	138S0811		ALL	Samsung alt to Murata	
376S1053	376S0604		ALL	Diodes alt to Fairchild	
152S00359	152S00253		ALL	Chillisin alt to Cyntec	
740S00027	740S0159		ALL	Bourns alt to Little Fuse	
371S0704	371S00077		ALL	NXP alt to Diodes	
138S00032	138S0831		ALL		
138S00049	138S0831		ALL		

					220uF 2.0V D-case, 128S00044 DQ
998-04070	998-04071		OFF	Hynix alt to SS	- T208
128S00010	128S00011		ALL		
128S00031	128S00011		ALL		
138S00084	138S00060		ALL		<rdar://problem/23118634> for IG <rdar://problem/23527737> for EG
155S00155	155S0441		OFF		(Stale; delete later after page sync)
155S00190	155S0897		ALL		
353S00107	353S3239		ALL		
353S00525	353S4471		ALL		
376S1193	376S00037		OFF		
740S00028	740S0118		ALL		
152S00369	152S00268		ALL	Cyntec w/ NEC	<rdar://problem/23405116> for IG <rdar://problem/23542193> for EG
128S0296	128S0487		ALL	NEC w/ pana	<rdar://problem/23422212> for IG <rdar://problem/23527282> for EG
128S00012	128S0487		ALL	NEC w/ Rohm	
155S00188	155S0275		ALL	Murata w/ Taiyo	<rdar://problem/23446936> for IG <rdar://problem/23542939> for EG
155S00018	155S0664		ALL	Murata w/ Taiyo	<rdar://problem/23447549> for IG <rdar://problem/23543068> for EG
152S00388	152S00182		ALL		<rdar://problem/23542023>
107S0240	107S0255		ALL		<rdar://problem/23520324>
128S00062	128S00067		ALL	NEC for Panasonic	150uF 6.3V B12
138S0660	138S0684		ALL		<rdar://problem/24316249>
155S00204	155S0731		ALL		<rdar://problem/24310837>

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
311S0271	311S00008		ALL	NXP w/ Diodes	(Stale; delete later after page sync) <rdar://problem/23117984> for IG <rdar://problem/24316367> for EG
197S00046	197S00036		ALL	Epson w/ TXC	<rdar://problem/23117749> for IG <rdar://problem/23543146> for EG
197S00047	197S00036		ALL	Kyocera w/ TXC	
197S00048	197S00036		ALL	Murata w/ TXC	
197S00053	197S00050		ALL	Kyocera w/ TXC	<rdar://problem/23117849> for IG <rdar://problem/23543858> for EG
197S00054	197S00050		ALL	NDK w/ TXC	
197S00055	197S00050		ALL	Murata w/ TXC	
311S0596	311S0593		ALL	NXP w/ Diodes	<rdar://problem/23118093> for IG <rdar://problem/23544024> for EG
107S0276	107S00020		ALL	Cyntec w/ TFT	<rdar://problem/23117951> for IG <rdar://problem/23542988> for EG
107S00021	107S0284		ALL	TFT w/ Yageo	<rdar://problem/23129685> for IG <rdar://problem/23519943> for EG
132S00012	132S0401		ALL	Taiyo w/ Murata&TDK	<rdar://problem/23118402> for IG <rdar://problem/23527525> for EG
152S00343	152S1682		ALL	NXP w/ Diodes	<rdar://problem/23541694> for IG <rdar://problem/23541871> for EG
107S00087	107S00029		ALL	TFT w/ Yageo	<rdar://problem/23121290> for IG <rdar://problem/23520039> for EG
128S00057	128S00018		ALL	NEC w/ Vishay	<rdar://problem/23363718> for IG <rdar://problem/23526361> for EG
128S00058	128S00018		ALL	NEC w/ Rohm	
128S0364	128S0264		ALL	Kemet w/ Panasonic	<rdar://problem/23366105> for IG <rdar://problem/23527232> for EG
138S0641	138S0700		ALL	Murata w/ SS&Taiyo	<rdar://problem/23118759> for IG <rdar://problem/23528188> for EG
138S0739	138S0706		ALL	NEC w/ Vishay	<rdar://problem/23118915> for IG <rdar://problem/23528364 for EG
138S0945	138S0706		ALL	NEC w/ Rohm	
152S00358	152S00208		ALL	Murata w/ Chillisin	<rdar://problem/23119390> for IG <rdar://problem/23542069> for EG
152S00389	152S00241		OFF	Cyntec w/ Vishay	<rdar://problem/23342644> for IG <rdar://problem/> for EG
152S00390	152S00265		OFF	Cyntec w/ Vishay	<rdar://problem/23342719> for IG <rdar://problem/> for EG
152S00400	152S1872		ALL	Murata w/ Cyntec	
152S1872	152S00361		ALL	Murata w/ Cyntec	<rdar://problem/23132240> for IG <rdar://problem/23542412> for EG
155S00034	155S0706		ALL	Taiyo w/ Murata	<rdar://problem/23118820> for IG <rdar://problem/23543018> for EG
371S00082	371S00046		ALL	On-Semi w/ Diodes	<rdar://problem/23341512> for IG <rdar://problem/23545301> for EG
376S00146	376S1061		ALL	NXP w/ Diodes	<rdar://problem/23341674> for IG <rdar://problem/23545469> for EG
353S00711	353S2073		ALL	On Semi w/ TI	<rdar://problem/23605939> for IG <rdar://problem/23605957> for EG
740S00019	740S00007		ALL	Bourns w/ Polytronics	<rdar://problem/23137505> for IG <rdar://problem/23545479> for EG
155S00189	155S0342		ALL	Murata w/ Taiyo	<rdar://problem/23117986> for IG <rdar://problem/23543015> for EG
132S0438	132S0428		ALL	Murata w/ Taiyo&TDK	<rdar://problem/23118548> for IG <rdar://problem/23527609> for EG
138S0714	138S0713		ALL	Murata w/ Samsung	<rdar://problem/23118842> for IG <rdar://problem/23528300> for EG
138S0715	138S0732		ALL	Murata w/ Samsung	<rdar://problem/23118873> for IG <rdar://problem/23528349> for EG
107S00086	107S00056		ALL	TFT w/ Cyntec	<rdar://problem/23121312> for IG <rdar://problem/23520074> for EG
138S0875	138S0678		ALL	Taiyo w/ Mur&SS	<rdar://problem/23129763> for IG <rdar://problem/23528106> for EG
138S0786	138S0705		ALL	Murata w/ Samsung	<rdar://problem/23129934> for IG <rdar://problem/23528216> for EG
155S0382	155S0659		ALL	Murata w/ TDK	<rdar://problem/23132624> for IG <rdar://problem/23543045> for EG
152S2052	152S1954		ALL	Taiyo w/ Cyntec	<rdar://problem/23135833> for IG <rdar://problem/23542478> for EG
152S2015	152S1958		ALL	Taiyo w/ Cyntec	<rdar://problem/23137154> for IG <rdar://problem/23542579> for EG
128S00055	128S00002		ALL	Kemet w/ Panasonic	<rdar://problem/23148659> for IG <rdar://problem/23526236> for EG
138S0748	138S0751		ALL	Murata w/ SS	<rdar://problem/23155052> for IG <rdar://problem/23528417> for EG
138S00102	138S0773		ALL	Murata w/ Taiyo	<rdar://problem/23155089> for IG <rdar://problem/23529046> for EG
138S0789	138S0941		ALL	Murata w/ SS	<rdar://problem/23155132> for IG <rdar://problem/23529142> for EG
107S00101	107S00005		ALL	Cyntec w/ Yageo	<rdar://problem/23193801> for IG <rdar://problem/23518872> for EG
107S00102	107S00017		ALL	Cyntec w/ Yageo	<rdar://problem/23194019> for IG <rdar://problem/23519914> for EG
107S00100	107S00057		ALL	Cyntec w/ TFT	<rdar://problem/23224358> for IG <rdar://problem/23528119> for EG
107S00103	107S00058		ALL	Cyntec w/ Yageo	<rdar://problem/23228523> for IG <rdar://problem/23520163> for EG
107S00104	107S00061		ALL	Cyntec w/ Yageo	<rdar://problem/23229217> for IG <rdar://problem/23520193> for EG
107S00105	107S00062		ALL	Cyntec w/ Yageo	<rdar://problem/23238371> for IG <rdar://problem/23520241> for EG
152S00403	152S00322		ALL	Murata w/ Chillisin	<rdar://problem/23341061> for IG <rdar://problem/23542282> for EG
353S00852	353S4262		ALL	TI w/ OnSemi	<rdar://problem/23341158> for IG <rdar://problem/23542282> for EG
138S00104	138S0978		ALL		<rdar://problem/23583487>
128S00069	128S00067		ALL	Rohm for Panasonic	150uF 6.3V B12 <rdar://problem/23527054>
138S0759	138S0762		ALL		<rdar://problem/23582324>
377S0077	377S0183		ALL		<rdar://problem/23640745>
152S00363	152S00048		ALL		<rdar://problem/23541533>
138S00111	138S00036		ALL		<rdar://problem/23546425>
138S00097	138S0750		ALL		<rdar://problem/23581953>
155S00203	155S0894		ALL		<rdar://problem/24285018>
116S00006	116S0175		ALL		<rdar://problem/23524119>
311S00104	311S00091		ALL		<rdar://problem/23640575>

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
311S00013	311S0508		ALL	Part will be stuffed in production	<rdar://problem/24316400>
311S00118	311S0489		ALL		<rdar://problem/27623384>
311S00072	311S0657		ALL		<rdar://problem/23595055>
311S00090	311S00028		ALL		<rdar://problem/23602138>
353S00750	353S00877		ALL		<rdar://problem/23545068>
353S00878	353S00599		ALL		<rdar://problem/23545040>
311S00105	311S0233		ALL		<rdar://problem/24316381>
353S00880	353S3452		ALL		<rdar://problem/23545099>
311S00007	311S0426		ALL		<rdar://problem/23597412>
128S0445	128S0392		ALL		<rdar://problem/23566873>
152S00415	152S00140		ALL		<rdar://problem/23766197>
128S0436	128S0392		ALL		<rdar://problem/23566873>
343S00135	343S00136		ALL	T208	
343S00137	343S00136		ALL	T208	
343S00138	343S00136		ALL	T208	
138S00105	138S00037		ALL		<rdar://problem/23640133>
152S00434	152S1829		ALL		<rdar://problem/23825631>
353S3527	353S3528		ALL		<rdar://problem/24492801>
353S3526	353S3528		ALL		<rdar://problem/24492801>
353S00135	353S00034		ALL		<rdar://problem/24534121>
353S2220	353S00034		ALL		<rdar://problem/24534121>
353S00769	353S4398		ALL		<rdar://problem/24534714>
353S00879	353S00754		ALL		<rdar://problem/23545008>
104S00012	155S0398		ALL		<rdar://problem/25180014>
353S4342	353S00854		ALL		<rdar://problem/23621422>
152S00543	152S00484		ALL		<rdar://problem/24780681>
371S00089	371S00085		ALL		<rdar://problem/24806090>
107S00111	107S00110		ALL		<rdar://problem/24968171>
335S00213	335S0888		ALL		<rdar://problem/24985900>
311S0437	311S00112		ALL		<rdar://problem/24747570>
377S0178	377S00031		ALL		<rdar://problem/25118595>
371S00091	371S00083		ALL		<rdar://problem/24827333>
197S00069	197S00068		ALL		<rdar://problem/24473517>
138S0698	138S00113		ALL		<rdar://problem/23528153>
152S00461	152S00112		ALL		<rdar://problem/24417973>
371S00074	371S0602		ALL		<rdar://problem/25919460>
197S00082	197S00081		ALL		
353S00991	353S00920		ALL		
131S00134	131S00041		ALL		<rdar://problem/24316117>

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Alternates BOM Table

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